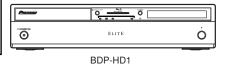
Pioneer sound.vision.soul

Service Manual



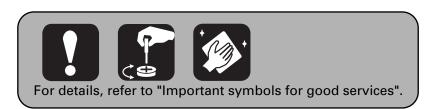
ORDER NO. RRV3466

BIU-ray Disc PLAYER

BDP-HD1

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Model	Туре	Power Requirement	Region No.	Remarks
BDP-HD1	KU/CA	AC120 V	1 BD Region A	



SAFETY INFORMATION



This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.

Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to causecancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 - Proposition 65

NOTICE

В

С

D

Ε

(FOR CANADIAN MODEL ONLY)

Fuse symbols — (fast operating fuse) and/or — (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE

(POUR MODÈLE CANADIEN SEULEMENT)

Les symboles de fusible — (fusible de type rapide) et/ou – (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

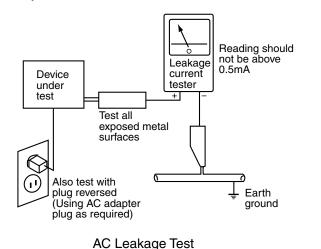
(FOR USA MODEL ONLY) -

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (waterpipe , conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a Δ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2

2

BDP-HD1

Α

В

С

D

Ε

CAUTION

This product is a class 1 laser product, but this product contains a laser diode higher than Class 1. To ensure continued safety, do not remove any covers or attempt to gain access to the inside of the product. Refer all servicing to qualified personnel.

CLASS 1 LASER PRODUCT APPAREIL Á LASER DE CLASSE 1

The following caution label appears on your unit. Location: inside of the unit

> CLASS 3B LASER RADIATION WHEN OPEN, AVOID EXPOSURE TO THE BEAM. CAUTION

RADIATIONS LASER DE CLASSE 3B QUAND OUVERT. ÉVITEZ TOUT EXPOSITION AU FAISCEAU. KLASSE 3B LASERSTRÂLING VED ÂBNING. UNDGÂ UDSÆTTELSE FOR STRÂLING. ATTENTION ANVARSEL

UNDA UUSET I ELSE FUN STRAING. KLASS 3B LASSRTÄÄLNING NÄR DENNA DEL ÄR ÖPPNAD. UNDVIK ATT UTSÄTTA DIG FÖR STRÅLEN. BEI GEÖFFNETER ABDEÖKUNG IST LASSRTÄRHLUNG DER KLASSE 3B IM GERTÄFUNKERS UVORHANDEN. AUGEN NICHT DEM LASERSTRAHL AUSSETZEN! VORSICHT

CUANDO SE ABRE HAY RADIACIÓN LÁSER DE CLASE 3B. EVITE LA EXPOSICIÓN A LOS RAYOS LÁSER.

AVATTAESSA ALTISTUT LUOKAN 3B LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN. VARO!

ここを開くと CLASS 3B の レーザ光が出ます。 ビームを直接見たり、触れたりしないこと。 注意

LASER DIODE CHARACTERISTICS FOR DVD: MAXIMUM OUTPUT POWER: 5 mW WAVELENGTH: 650 nm

WAVELENGTH: 780 nm

MAXIMUM OUTPUT POWER: 7 mW

WARNING!

THE AEL (ACCESSIBLE EMISSION LEVEL) OF THE LASER POWER OUTPUT IS LESS THAN CLASS 1 BUT THE LASER COMPONENT IS CAPABLE OF EMITTING RADIATION EXCEEDING THE LIMIT FOR CLASS 1.

A SPECIALLY INSTRUCTED PERSON SHOULD DO SERVICING OPERATION OF THE APPARATUS.

LABEL CHECK

CAUTION

CLASS 3B LASER RADIATION WHEN OPEN,

AVOID EXPOSURE TO THE BEAM.

RADIATIONS LASER DE CLASSE 3B QUAND OUVERT. ATTENTION

ÉVITEZ TOUT EXPOSITION AU FAISCEAU.

KLASSE 3B LASERSTRÅLING VED ÅBNING. UNDGÅ UDSÆTTELSE FOR STRÅLING. ADVARSEL

KLASS 3B LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD. VARNING

undvik att utsätta dig för strålen.

BEI GEÖFFNETER ABDECKUNG IST LASERSTRAHLUNG DER KLASSE 3B IM GERÄTEINNEREN VORHANDEN. **VORSICHT**

AUGEN NICHT DEM LASERSTRAHL AUSSETZEN!

PRECAUCIÓN CUANDO SE ABRE HAY RADIACIÓN LÁSER DE CLASE 3B. EVITE LA EXPOSICIÓN A LOS RAYOS LÁSER.

VARO! AVATTAESSA ALTISTUT LUOKAN 3B LASERSÄTEILYLLE. älä katso säteeseen.

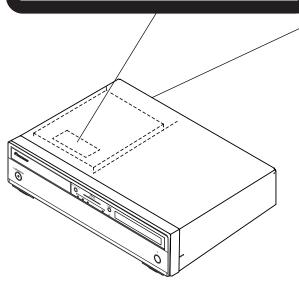
ここを開くと CLASS 3B の レーザ光が出ます。 注意

ビームを直接見たり、触れたりしないこと。

CLASS 1 LASER PRODUCT

(Printed on the Rear Panel)

FOR CD:



APPAREIL A LASER DE CLASSE 1

BDP-HD1

3

5

DRW2277-A

In this manual, procedures that must be performed during repairs are marked with the below symbol. Please be sure to confirm and follow these procedures.

1. Product safety



Please conform to product regulations (such as safety and radiation regulations), and maintain a safe servicing environment by following the safety instructions described in this manual.

① Use specified parts for repair.

Use genuine parts. Be sure to use important parts for safety.

2 Do not perform modifications without proper instructions.

Please follow the specified safety methods when modification(addition/change of parts) is required due to interferences such as radio/TV interference and foreign noise.

3 Make sure the soldering of repaired locations is properly performed.

When you solder while repairing, please be sure that there are no cold solder and other debris. Soldering should be finished with the proper quantity. (Refer to the example)

Make sure the screws are tightly fastened.

Please be sure that all screws are fastened, and that there are no loose screws.

5 Make sure each connectors are correctly inserted.

Please be sure that all connectors are inserted, and that there are no imperfect insertion.

6 Make sure the wiring cables are set to their original state.

Please replace the wiring and cables to the original state after repairs. In addition, be sure that there are no pinched wires, etc.

Make sure screws and soldering scraps do not remain inside the product.

Please check that neither solder debris nor screws remain inside the product.

There should be no semi-broken wires, scratches, melting, etc. on the coating of the power cord.

Damaged power cords may lead to fire accidents, so please be sure that there are no damages. If you find a damaged power cord, please exchange it with a suitable one.

(9) There should be no spark traces or similar marks on the power plug.

When spark traces or similar marks are found on the power supply plug, please check the connection and advise on secure connections and suitable usage. Please exchange the power cord if necessary.

10 Safe environment should be secured during servicing.

When you perform repairs, please pay attention to static electricity, furniture, household articles, etc. in order to prevent injuries. Please pay attention to your surroundings and repair safely.

2. Adjustments



C

D

To keep the original performance of the products, optimum adjustments and confirmation of characteristics within specification. Adjustments should be performed in accordance with the procedures/instructions described in this manual.

3. Lubricants, Glues, and Replacement parts



Use grease and adhesives that are equal to the specified substance. Make sure the proper amount is applied.

4. Cleaning



For parts that require cleaning, such as optical pickups, tape deck heads, lenses and mirrors used in projection monitors, proper cleaning should be performed to restore their performances.

5. Shipping mode and Shipping screws



To protect products from damages or failures during transit, the shipping mode should be set or the shipping screws should be installed before shipment. Please be sure to follow this method especially if it is specified in this manual.

BDP-HD1 3 ■

■ 6 **■** 7 **■** 8

CONTENTS

SAFETY INFORMATION	2
1. SPECIFICATIONS	6
2. EXPLODED VIEWS AND PARTS LIST	8
2.1 PACKING	8
2.2 EXTERIOR SECTION	10
2.3 FRONT PANEL SECTION	
3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM	14
3.1 BLOCK DIAGRAM	14
3.2 POWER BLOCK	
3.3 OVERALL WIRING DIAGRAM	16
3.4 MAIN ASSY 1/7	18
3.5 MAIN ASSY 2/7	
3.6 MAIN ASSY 3/7	
3.7 MAIN ASSY 4/7	
3.8 MAIN ASSY 5/7	28
3.9 MAIN ASSY 6/7	
3.10 MAIN ASSY 7/7	
3.11 FLKY and PSWB ASSYS	
3.12 AUJB ASSY 1/2	
3.13 AUJB ASSY 2/2	
3.14 SRJB and WRPB ASSYS	
3.15 SYPS ASSY	
3.16 WAVEFORMS	
4. PCB CONNECTION DIAGRAM	
4.1 AUJB ASSY	
4.2 MAIN ASSY	
4.3 FLKY and PSWB ASSYS	
4.4 SRJB and WRPB ASSYS	
4.5 SYPS ASSY	
5. PCB PARTS LIST	
6. ADJUSTMENT	
6.1 NECESSARY ADJUSTMENT POINTS	
6.2 ID NUMBER AND DATA SETTING	
6.3 FIRMWARE UPDATE	
7. GENERAL INFORMATION	
7.1 DIAGNOSIS	
7.1.1 SERVICE KEY INPUT	
7.1.2 SCREEN INDICATION FOR SERVICING	
7.1.3 HOW TO MEASURE THE ERROR RATE	
7.1.4 TROUBLE SHOOTING	
7.2 DISASSEMBLY	
7.3 PARTS	
7.3.1 IC	
7.4 DISC / CONTENT FORMAT PLAYBACK COMPATIBILITY	
8. PANEL FACILITIES	.137

Ε

В

1. SPECIFICATIONS

Specifications

General	Audio output
SystemBD Player (BD-ROM, DVD-Video, DVD-R/RW,	Output level .
network file playback)	Number of ch
Power requirements	Jacks
Power consumption (standby) 0.5 W	Audio charac
Weight 6.3 kg (13 lb 15 oz)	Frequency res
Dimensions	0.15.1
(16 $^{9/16}$ in. (W) x $4^{5/8}$ in. (H) x $14^{3/16}$ in. (D))	S/N ratio Dynamic rang
Operating temperature+5 °C to +35 °C	Total harmoni
Operating humidity	Wow and flutt
HDMI output (no condensation)	
•	
HDMI output	Digital outpu
Component Video output (Y, PB, PR)	Optical digital Coaxial digita
Output level	Coaxiai digita
PB, PR: 0.7 Vp-p (75 Ω)	Other termin
Jacks RCA jacks	LAN terminal
S-Video output	Control in
Y (luminance) - Output level	IR in
C (color) - Output level	
Jack 5- Video jack	Accessories
Video output	Stereo audio
Output level	Video cable .
Jack RCA jack	Power cable
Audio output (1 stereo pair)	Remote contr AA/LR6 batte
Output level During audio output	Warranty card
200 mVrms (1 kHz, –20 dB)	These operati
Number of channels	T :: ::
- The state of the	The specification

Audio output (multi-channel / L, R, C, SW, LS, RS) Output level
Number of channels
Audio characteristics Frequency response
S/N ratio
Digital output Optical digital output Optical digital jack Coaxial digital output RCA jack
Other terminals LAN terminal Ethernet jack 10 BASE-T/100 BASE-TX Control in Minijack (3.5 ø) IR in Minijack (3.5 ø)
Accessories Stereo audio cable 1 Video cable 1 Power cable 1 Remote control 1 AA/LR6 batteries 2 Warranty card 1 These operating instructions

The specifications and design of this product are subject to change without notice.

This product includes FontAvenue[®] fonts licenced by NEC corporation. FontAvenue is a registered trademark of NEC Corporation.

6

D

BDP-HD1

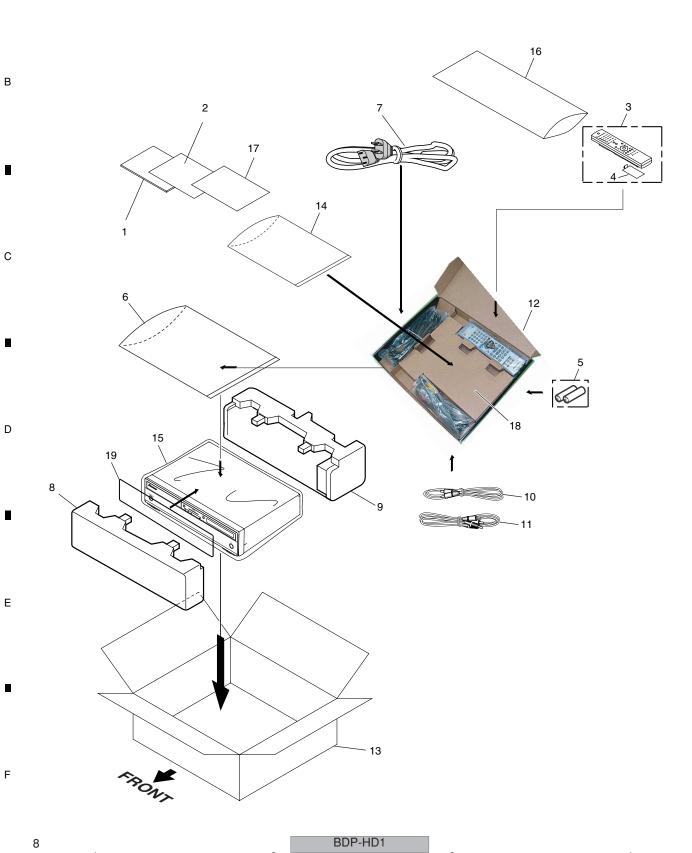
5 6 7 8 Α В С D Ε BDP-HD1 5 8

2. EXPLODED VIEWS AND PARTS LIST

NOTES: ● Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The \triangle mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- Screws adjacent to ▼ mark on product are used for disassembly.
- For the applying amount of lubricants or glue, follow the instructions in this manual. (In the case of no amount instructions, apply as you think it appropriate.)

2.1 PACKING



PACKING parts List

Mark	<u>No.</u>	<u>Description</u>	Part No.	
	1	Instruction Manual	VRB1410	
		(English, French)		
NSP 2		Warranty Card	ARY1026	
	3	Remote Control Unit	VXX3101	
	4	Battery Cover	AZN7933	
NSP 5		Bettery (R6P, AA)	AEX1025	
	6	Nonwoven Fabric Bag	VHL1108	
\triangle	7	AC Power Cord	ADG7061	
	8	FRONT Pad (PS)	VHA1411	
	9	REAR Pad (PS)	VHA1412	
	10	Video cable	VDE1065	
	11	Stereo audio cable	VDE1064	
	12	Accessory Box	VHC1169	
	13	Packing Case	VHG2711	
NSF	14	Polyethylene Bag(230x340)	Z21-038	
	15	Mirror Sheet	VHL1006	
	16	Polyethylene Bag	VHL1051	
	17	User Card	ARY1176	
	18	Patation Plate (Paper)	VHC1170	
	19	Nonwoven Cloth Cover	VHL1116	

В

D

Е

-

		5	6			7	8		
EXTE Mark		OR SECTION parts List Description	Part No.	<u>Mark</u> !	No.	Description	Part No.		
IVICIA		-		<u></u> .	140.	<u> </u>	1 411		
	1	MAIN ASSY	VXX3151	NCD	C 1	ID Label ACCV	\/\/\\/1013		
	2	AUJB ASSY	VWG2578	NSP		ID Label ASSY	VXW1013		Α
	3	WRPB ASSY	VWG2591		52	Connector ASSY	PF12PP6D22		ĺ
	4	SRJB ASSY	VWG2579		53	Connector ASSY	PF13PP-D25		
	5	Housing ASSY (4P)	VKP2388		54	Housing ASSY (ATA)	VKP2384		
	6	Housing ASSY (4P)	VKP2387						
\triangle	7	AC Inlet ASSY	ADX7523						_
\triangle	8	SYPS ASSY	VWR1402						
	9	Drive ASSY BDR101A	VXX3148			Service AUSR ASSY	VXX3152		
	10	Filter	CTX1054	NSP		1AUSR ASSY 2AUJB ASSY	VWM2394 VWG2578		
	11	Hold Spring	VBK1168			2WRPB ASSY	VWG2591		В
	12	Rubber Foot	VEB1349			2SRJB ASSY	VWG2579		
	13	Radiation Sheet	VEB1349 VEB1360			201 105 7.00 1	***************************************		
		SYPS Rubber							
	14		VEB1386						
	15	Rubber Spacer1	VEB1387						
	16	Rubber Spacer2	VEB1388						
	17	Spacer S	VEB1392						
	18	Spacer R	VEB1393						
	19	Cushion	VEB1395						ļ
	20	Card Spacer	VEC1708						С
NSP	21	Clamp	VEC2418						
	22	Styling Sheet	VEC2527						
	23	Barrier	VEC2526						
	24	Gasket	VEC2528						1
	25	Front Cushion	VEC2538						
	26	Small Clamp	VEC2541						ļ
	27	Gasket	VEC2552						ļ
	28	Bonnet Case S	VXX3053						ļ
	28 29	Rear Panel	VNA2867						ļ
NSP		PCB Base	VNE2378						D
									ļ
NSP		Sub Chassis	VNE2389						1
NSP		Writer Stay L	VNE2390						ļ
NSP		Writer Stay R	VNE2391						. !
NSP		Front Stay	VNE2393						
NSP	35	Layer Plate	VNE2394						
NSP	36	PCB Stay	VNE2399						
	37	Heatsink	VNH1078						
	38	Insulator	VNK5794						_
	39	Stopper	VNK6140						Е
	40	Ferrite Core	VTX1002						
NSP	41	Base Chassis ASSY	VXA2743						
	42	Screw	AMZ30P060FTC						
	43	Screw	AMZ30P060FTC						
	44	Screw	BBZ30P060FBN						
	45	Screw	BBZ30P060FCC						
	46	Screw	BBZ30P060FTC						
	47	Screw	BPZ30P080FCC						5
	48	Screw	CBZ30P080FCC						F
NICD	49	Screw	PCZ30P060FCC						
NSP	50	Serial Label S	VRW2017	DDD 11D1		_			
		5 -	6	BDP-HD1		7 -	8	11	

a 6 **b** 7 **a** 8

Α

В

D

Е

F

26 Refer to "2.2 EXTERIOR SECTION.A" В 30 16 28 20 NON-CONTACT SIDE CONTACT SIDE

12

BDP-HD1

FRONT PANEL SECTION parts List

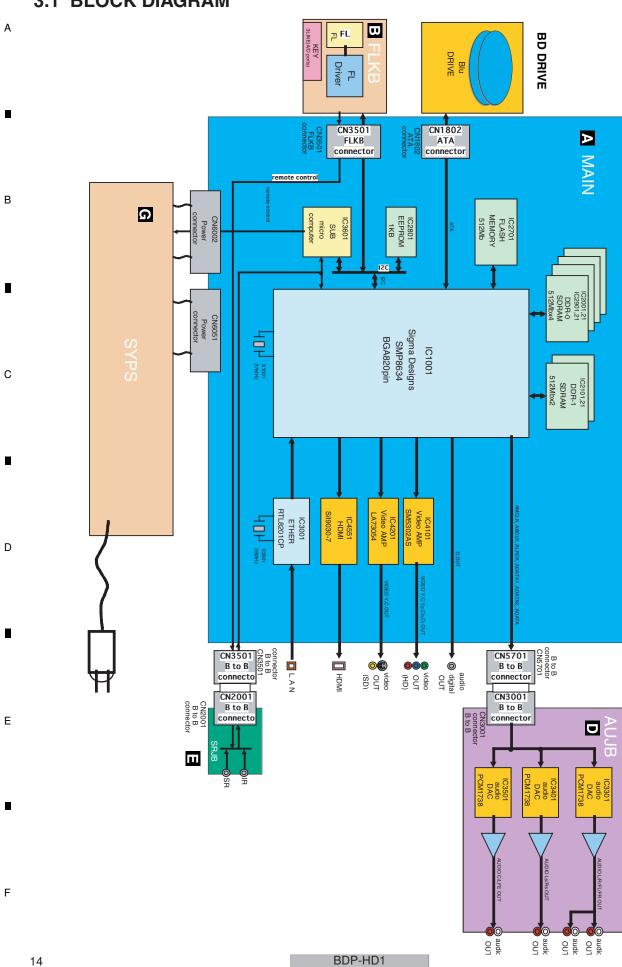
<u>Mark</u>	<u>No.</u>	<u>Description</u>	Part No.
	1	FLKY ASSY	VWG2559
	2	PSWB ASSY	VWG2560
	3	Magnet Holder ASSY	AEC1077
	4	Name Plate B	PAN1376
	5	Rubber Sheet	VEB1372
	6	Tray Sheet	VEC2502
	7	FL Filter	VEC2534
	8	Spacer	VEC2543
	9	Damper Spacer	VEC2546
	10	Door Panel B	VNB1054
	11	Magnet Catcher	VNE2388
	12	Illumi Lens A	VNK5783
	13	Power Key 1	VNK5790
	14	LED Lens	VNK5792
	15	Door Base	VNK5918
	16	Tray Panel	VNK5920
	17	Panel Base	VNK5945
	18	Key Top	VNK5946
	19	Door Ring	VNK5947
	20	FL Lens	VNK5948
	21	Key Top A	VNK5949
	22	Main Key	VNK5997
	23	Front Panel	VNK6015
	24	Menu Key	VNK6089
	25	Damper ASSY	VXA2504
	26	Screw	BPZ30P080FBN
	27	Hologram Label	VRW2264
NSP	28	Energy Star Label	AAX8022
NSP	29	Pop Label	VRW2329
	30	Flexible Cable (6P)	VDA2071
	31	Flexible Cable (28P)	VDA2152
		Service FLKB ASSY	VXX3153
NSP		1FLKB ASSY	VWM2357
		2FLKY ASSY	VWG2559
		2PSWB ASSY	VWG2560

В

D

Ε

3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM 3.1 BLOCK DIAGRAM



5

BDP-HD1

6

7

6

Α

8

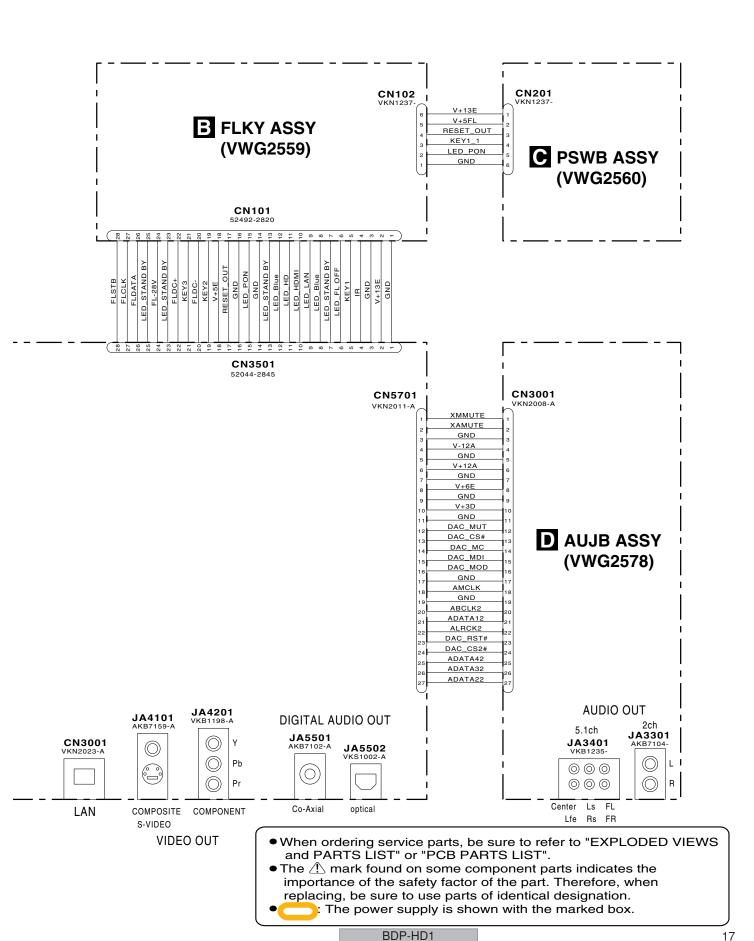
В

С

D

Ε

F

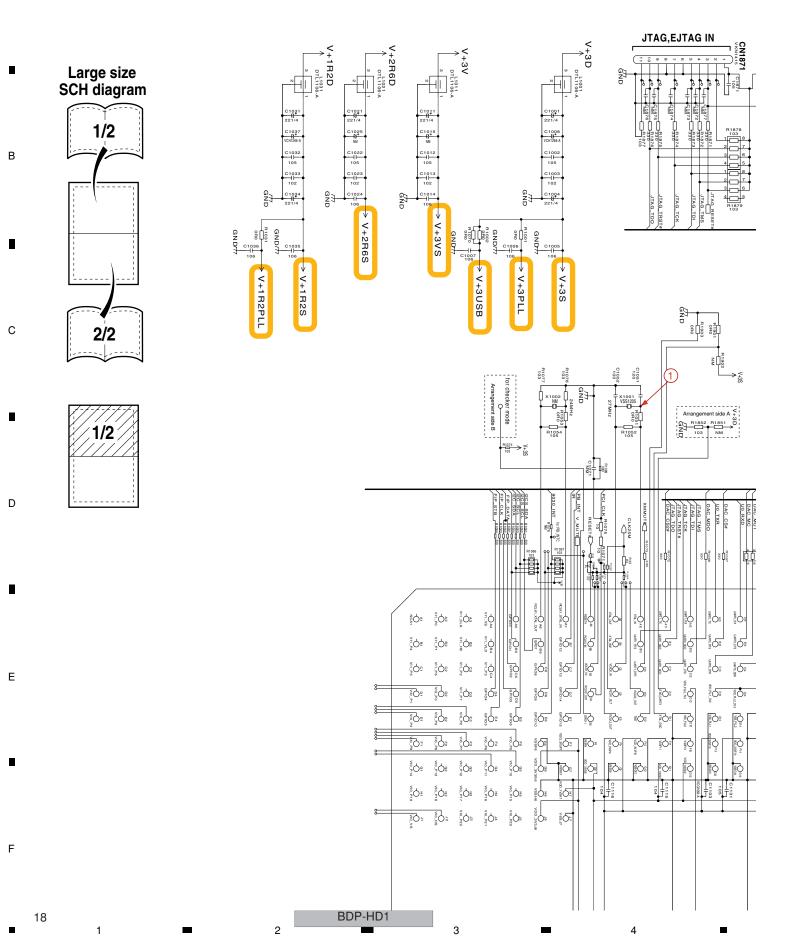


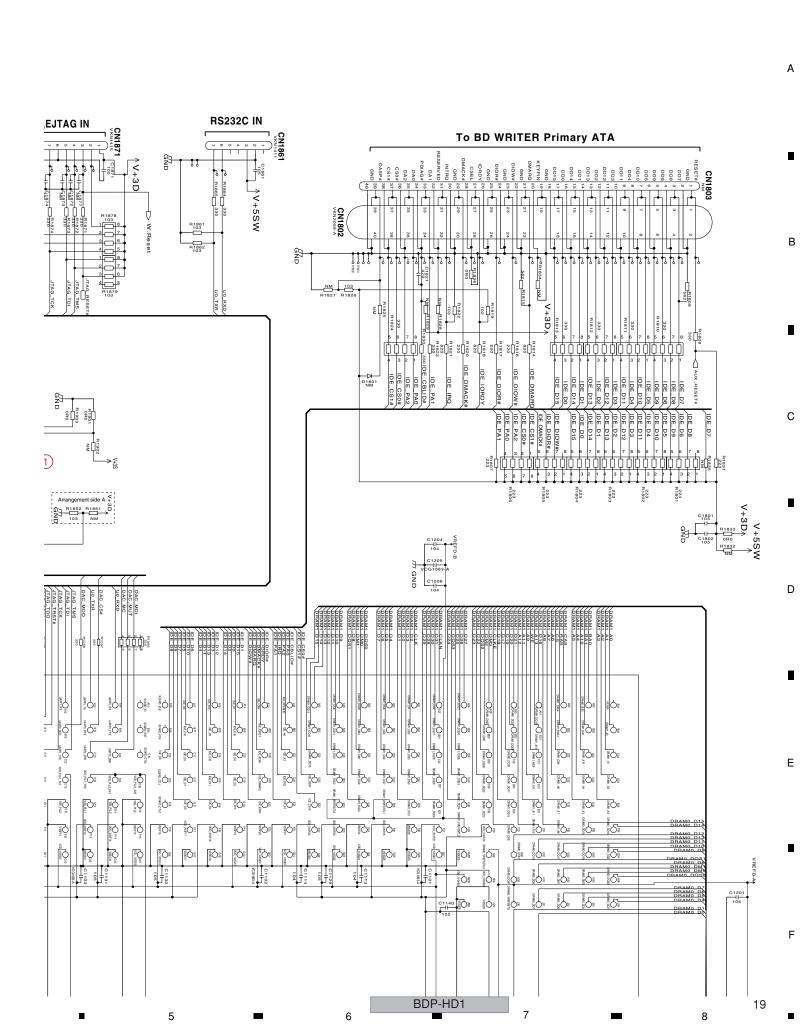
В

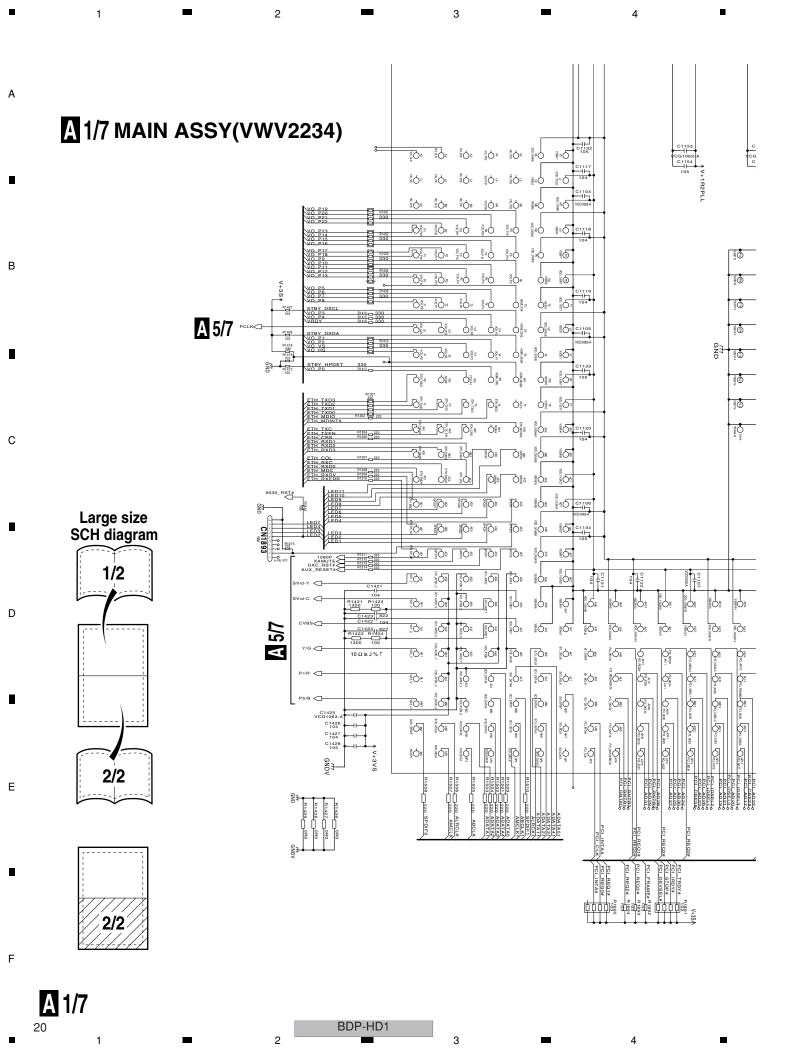
D

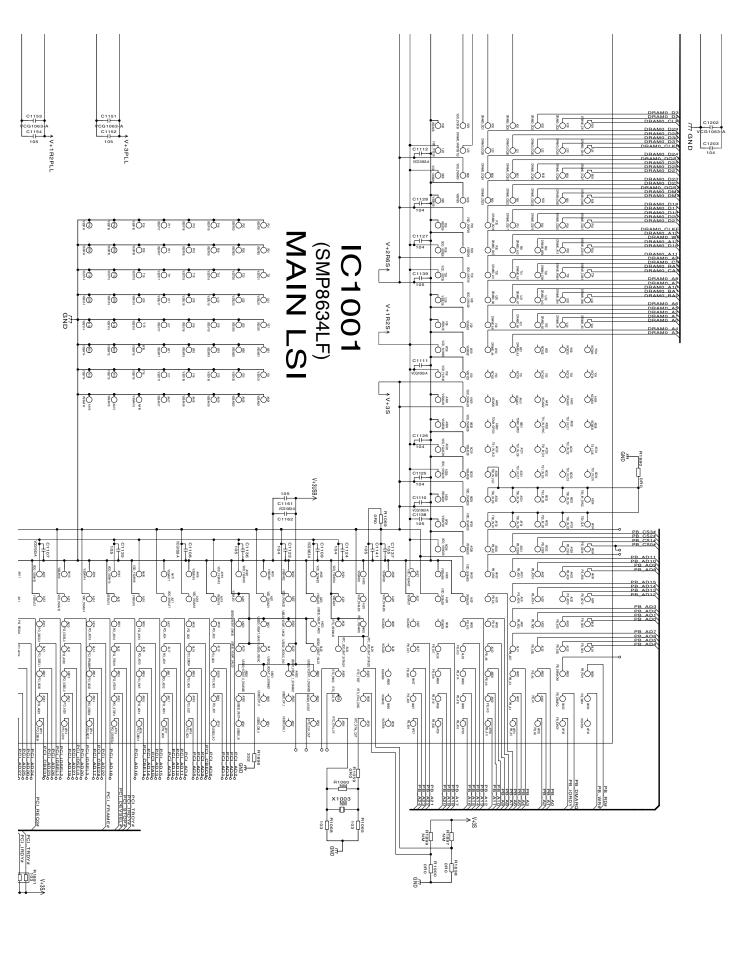
Ε

1/7 MAIN ASSY(VWV2234)









5

5

A 1/7

В

С

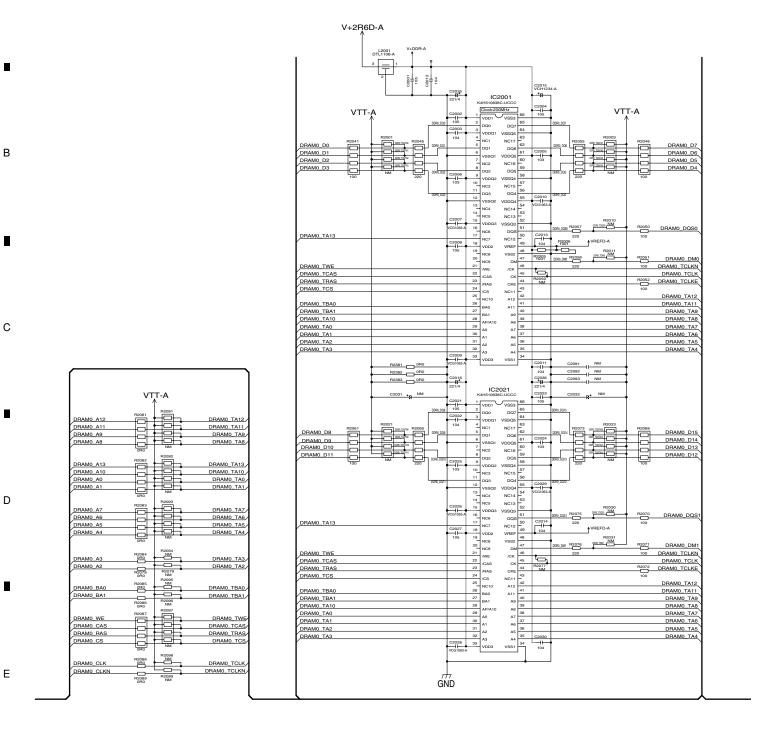
D

Ε

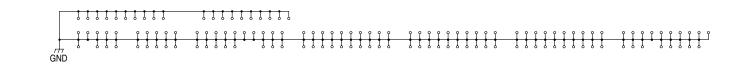
BDP-HD1

3.5 MAIN ASSY 2/7

A 2/7 MAIN ASSY(VWV2234)



3

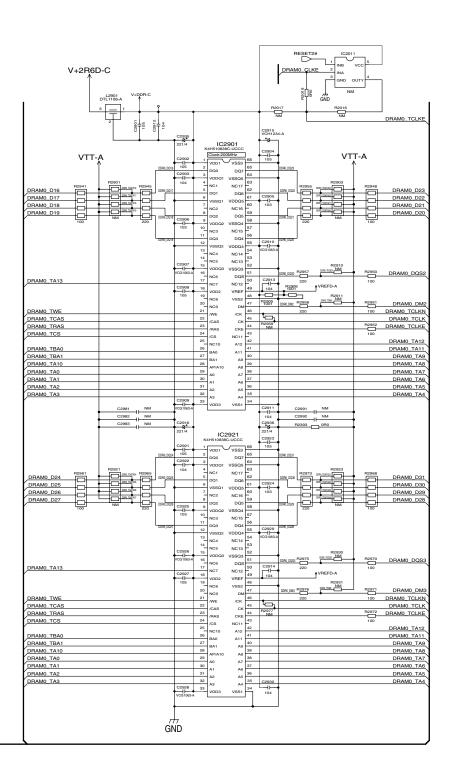


A 2/7

F

2

BDP-HD1



7

5

5

Α

8

В

С

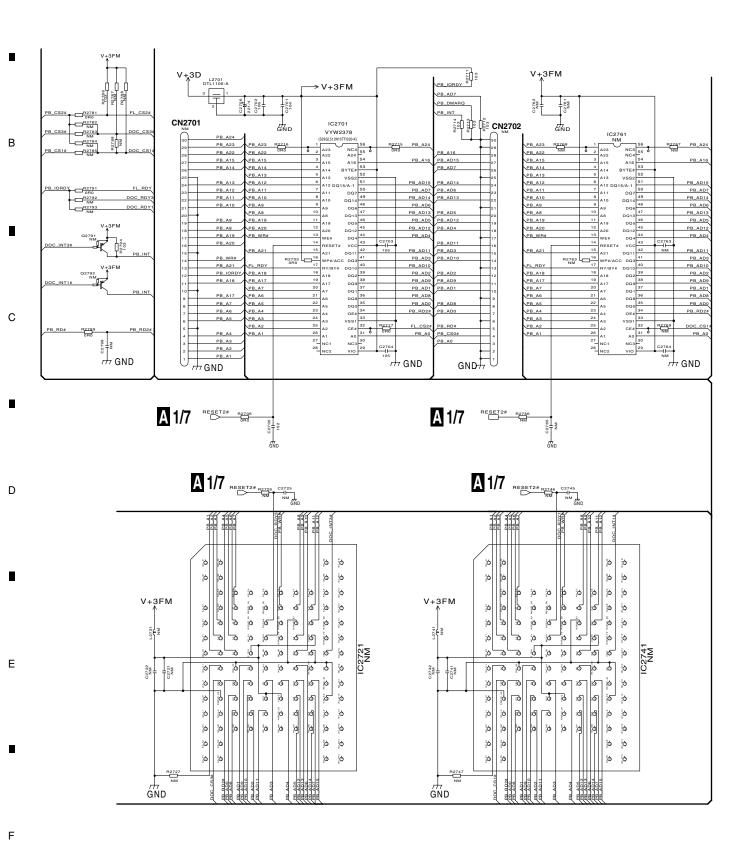
D

Ε

F

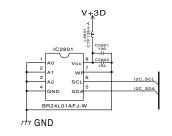
A 2/7 23

A 3/7 MAIN ASSY(VWV2234)



A 3/7

BDP-HD1



Α

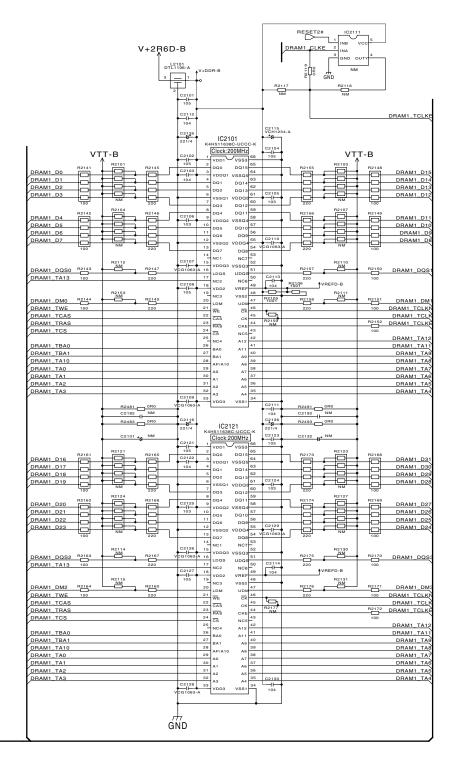
В

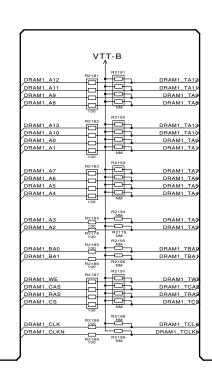
С

D

Ε

7





5

6

A 3/7

BDP-HD1

6

7

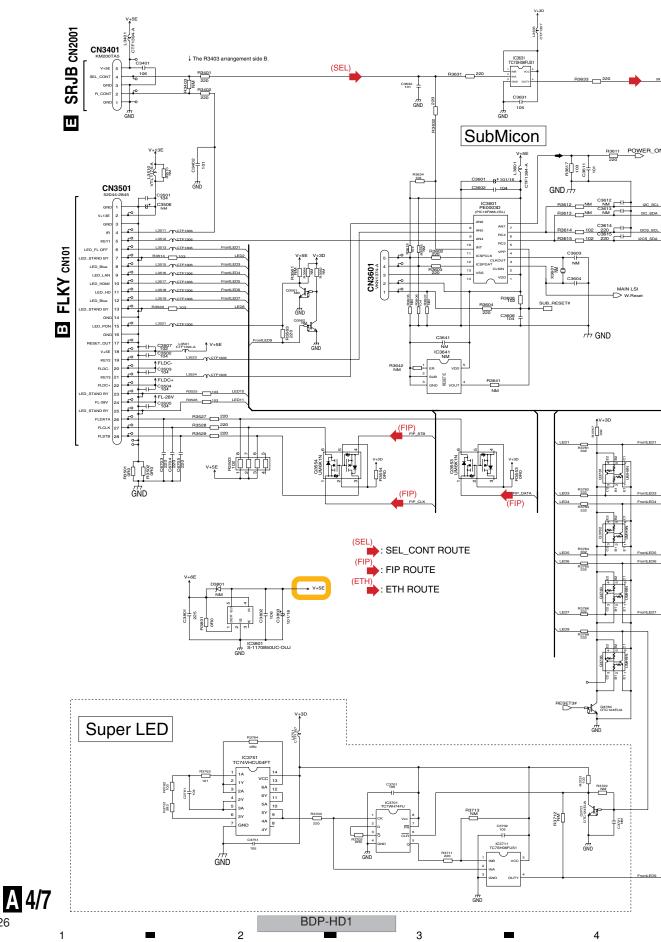
8

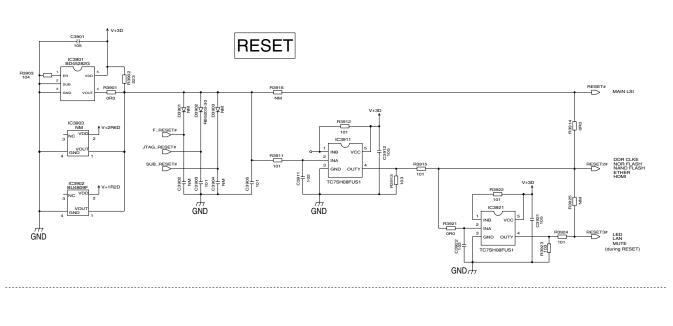
25

D

Е

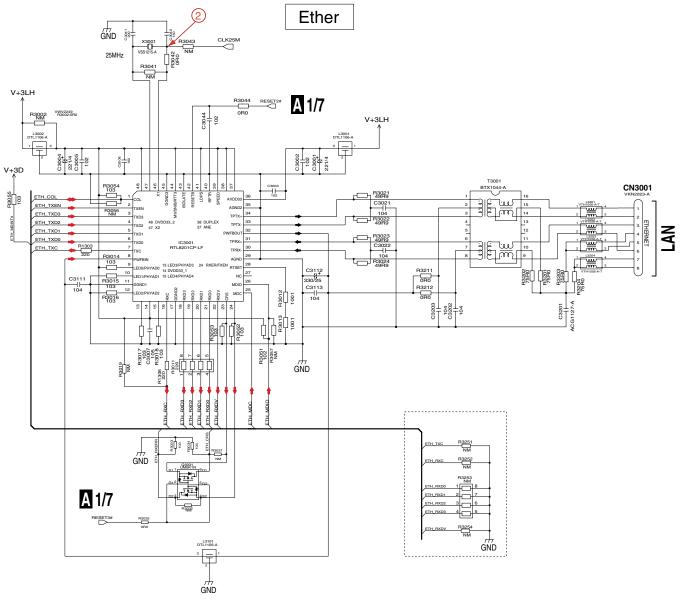
A 4/7 MAIN ASSY(VWV2234)





5

5



A 4/7

8

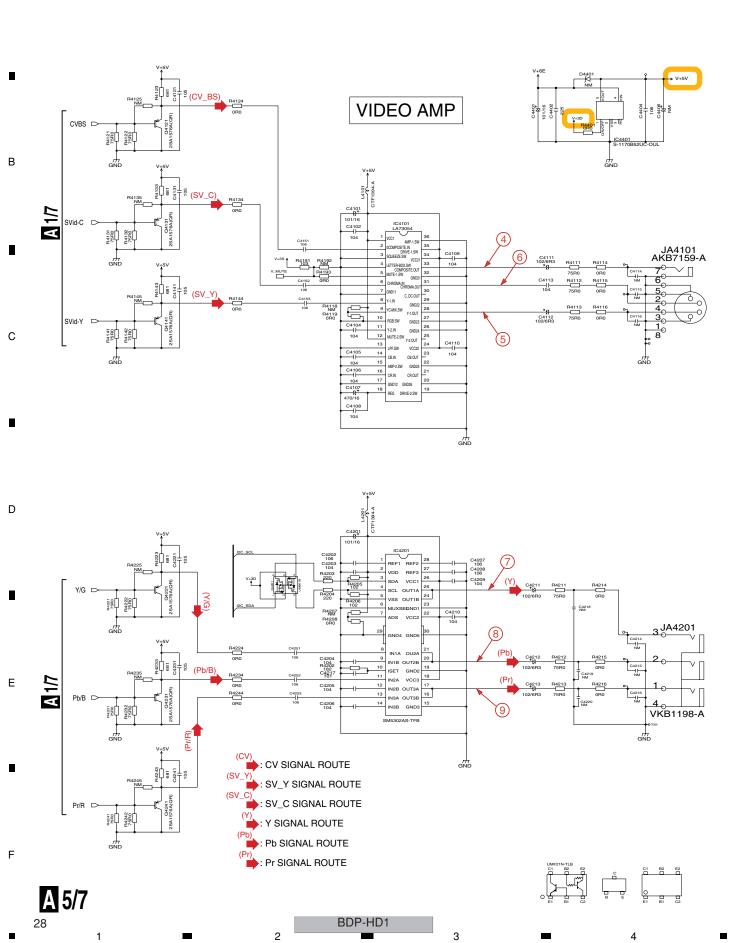
В

С

Е

3.8 MAIN ASSY 5/7

A 5/7 MAIN ASSY(VWV2234)



HDMI

6

5

5

7

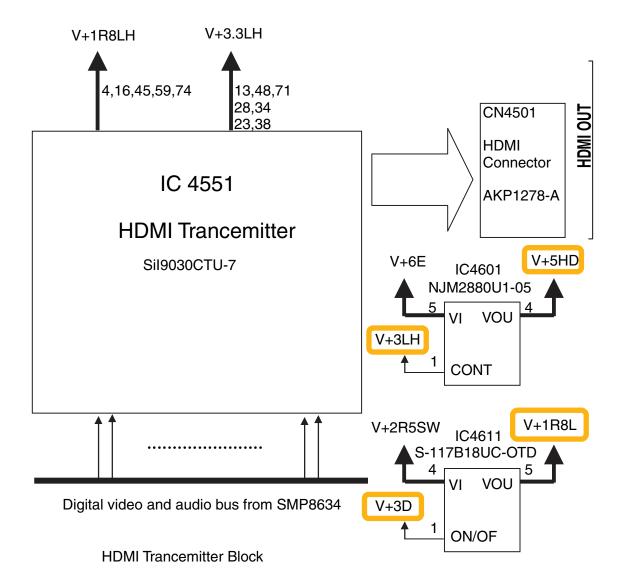
8

В

С

D

Ε



A 5/7

7 -

7

BDP-HD1

3.9 MAIN ASSY 6/7

В

С

D

Е

A 6/7 MAIN ASSY(VWV2234)

AUDIO I/F

R5718 NM CN5701 R5712 OR0 R5714 OR0 R5719 NM R5715 OR0 ADATA42 R5102 NM R5716 _____ 0R0 ADATA41 R5103 0R0 R5702 OR0 ADATA4 R5104 NM R5703 OR0 ALRCK2 R5105 OR0 ADATA3 R5106 NM ABCLK2 R5705 OR0 ADATA21 R5107 0R0 ADATA2 R5108 NM to AUJB CN3001 R5110 NM DAC_MDI R5708 OR0 R5111 0R0 DAC_MC R5709 OR0 ABCLK1 R5113 0R0 DAC_CS# R5710 OR0 R5114 NM AMCLK R5116 ORO V+6E 1573175-A V+12A ↑ C5703 C5711 C5711 GND/// V-12A ↑ C5802

A 6/7

BDP-HD1

-

AUDIO Digital

7

8

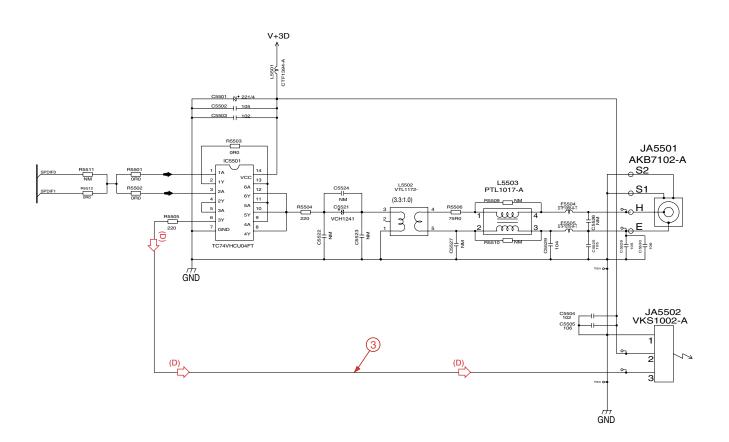
В

С

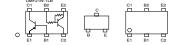
D

Ε

6



(D): AUDIO (DIGITAL) SIGNAL ROUTE



5

5

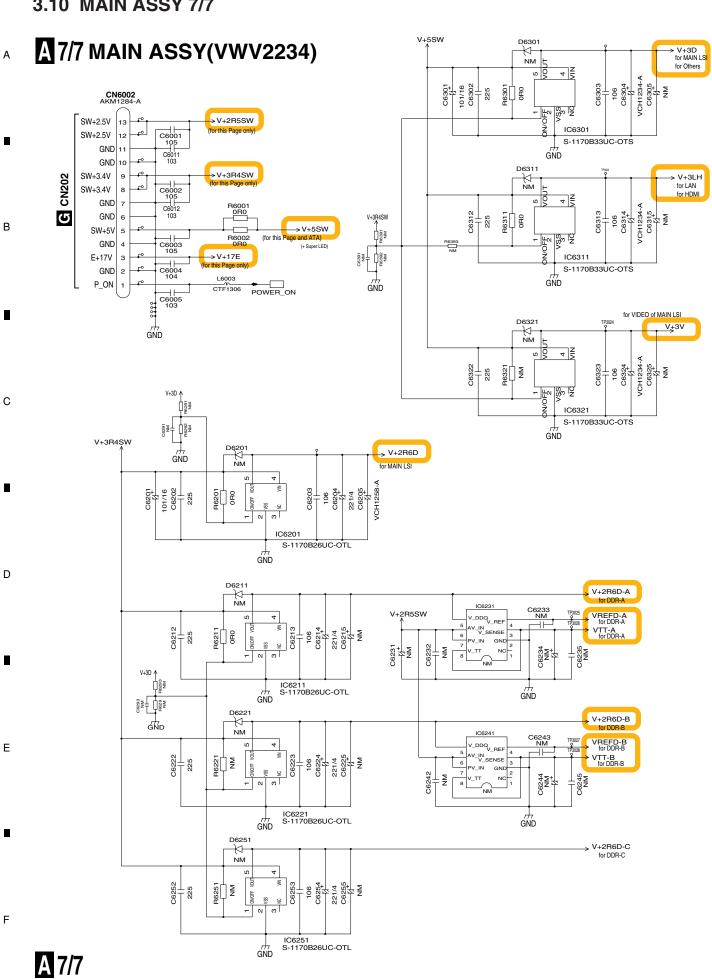
A 6/7

BDP-HD1

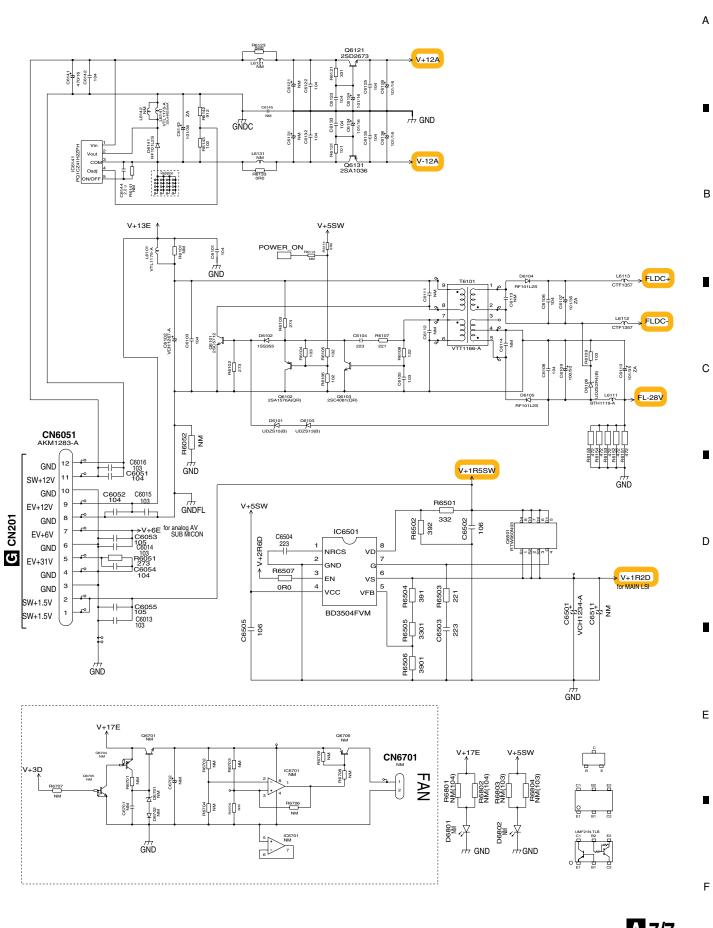
F

2

3



BDP-HD1



A 7/7

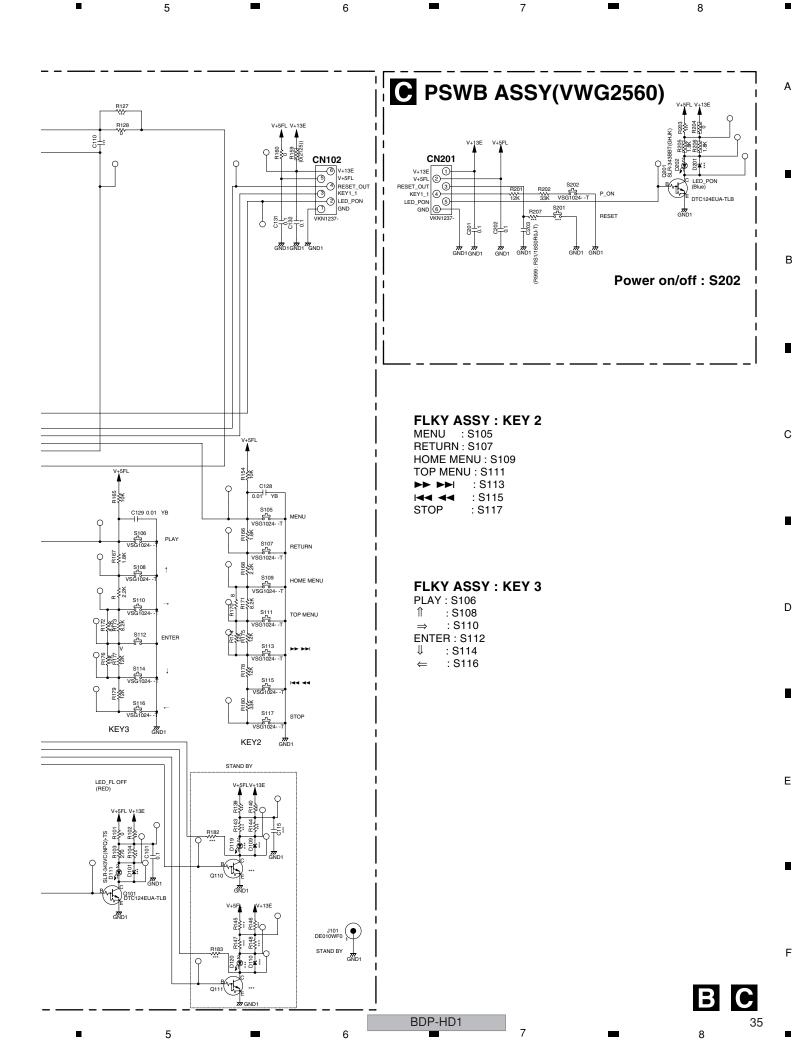
BDP-HD1

В

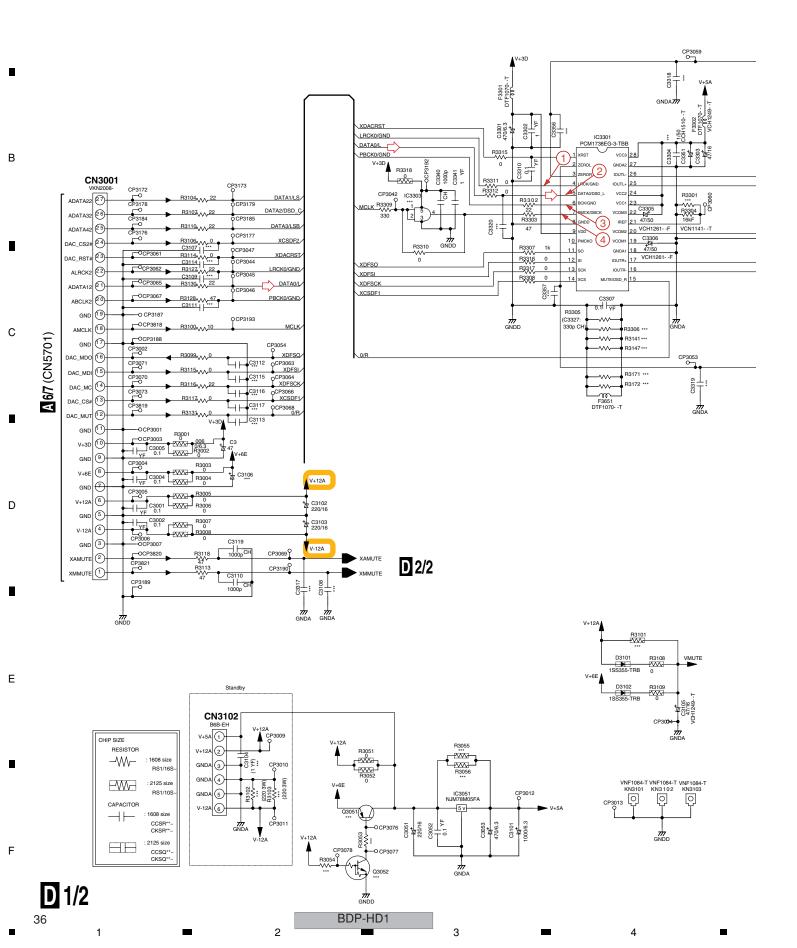
С

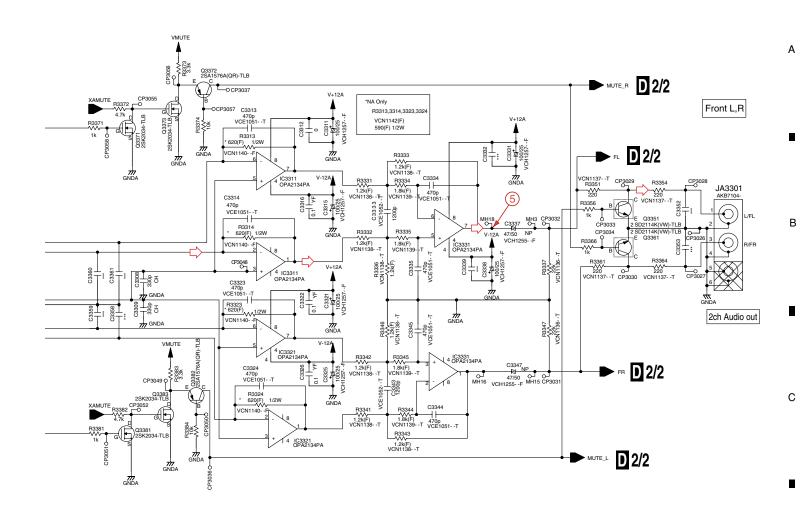
D

Ε



1/2 AUJB ASSY(1/2)(VWG2578)





7

8

: AUDIO SIGNAL ROUTE



D 1/2

D

Е

BDP-HD1

7

8

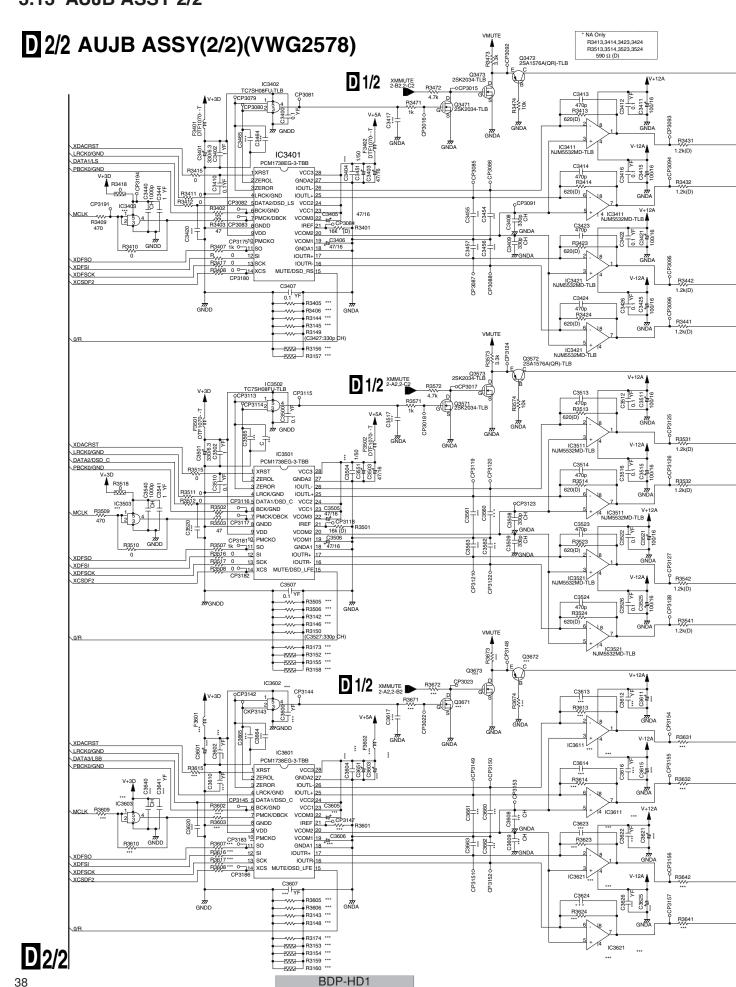
Α

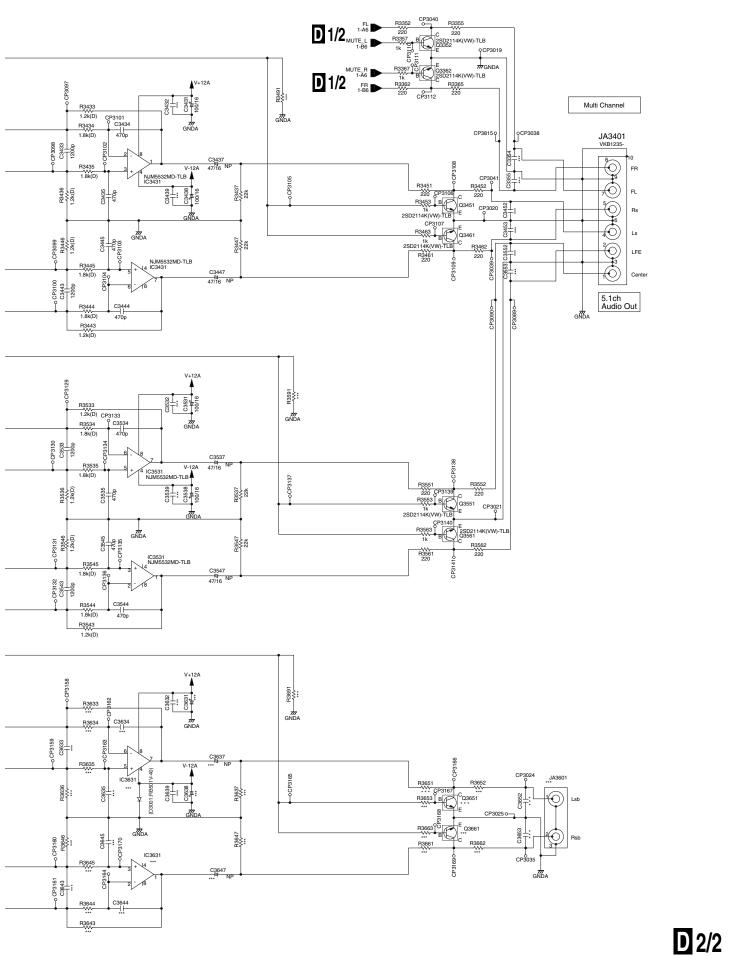
В

С

D

Ε





5

7

8

Α

В

С

D

Ε

BDP-HD1

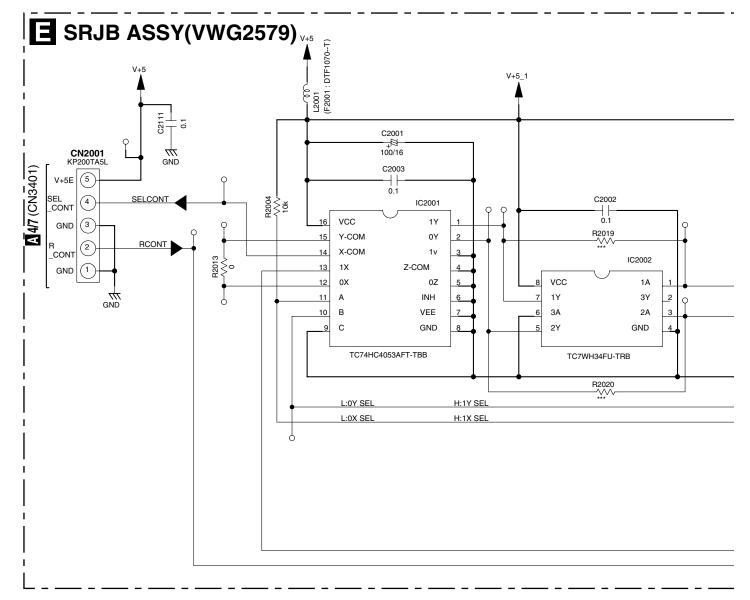
5

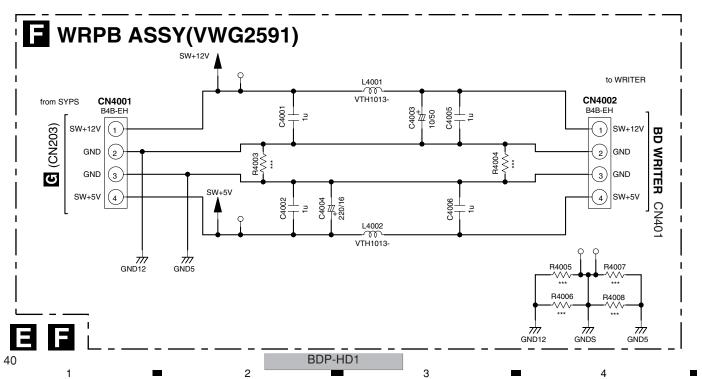
6

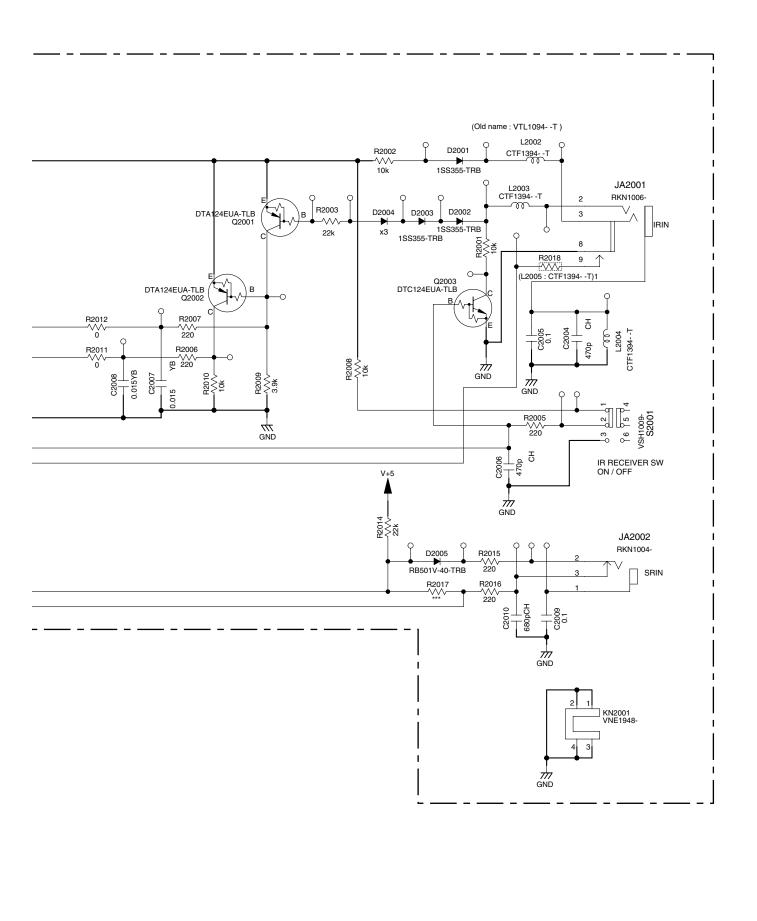
С

D

Ε







5

5

7

8

Α

В

С

D

Е

Ξ

BDP-HD1

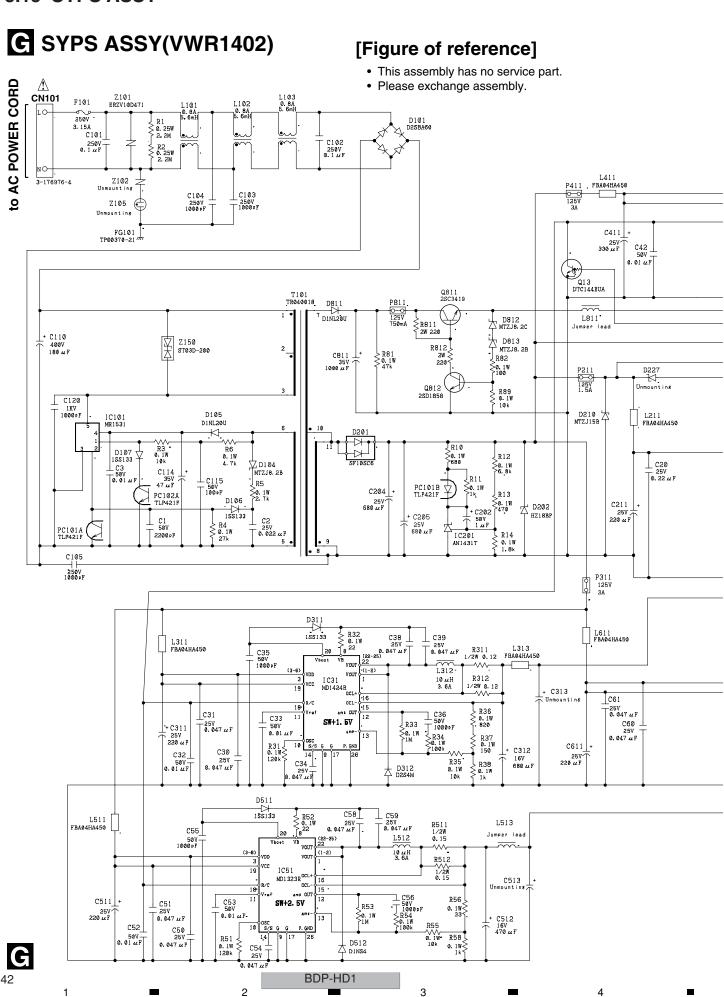
= 8

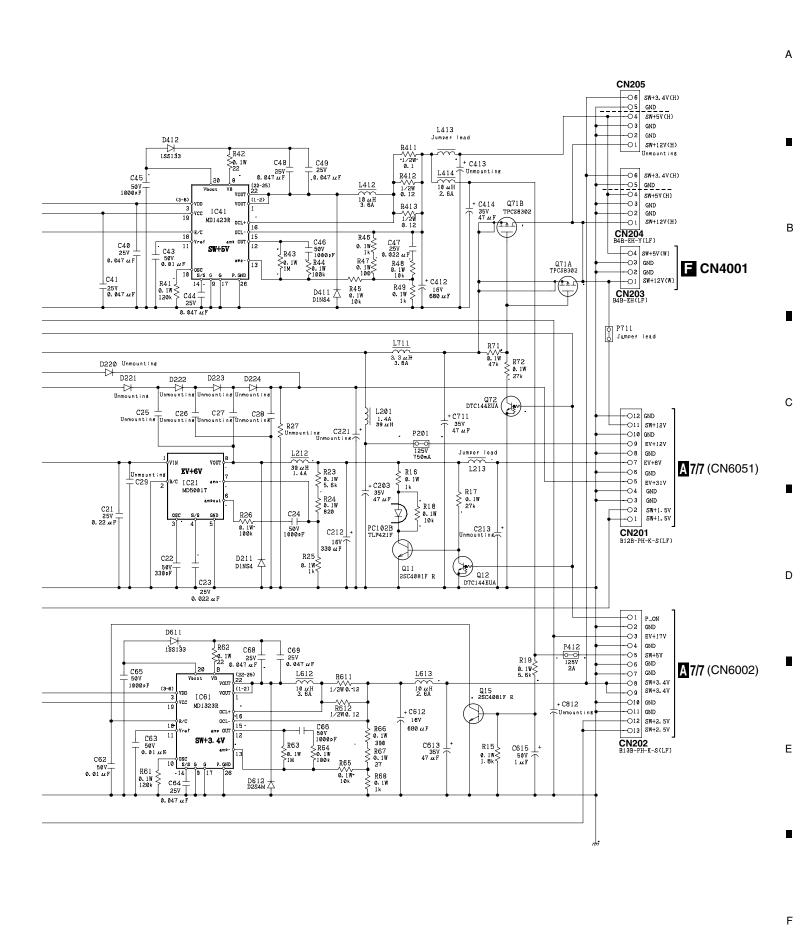
В

С

D

Ε





G

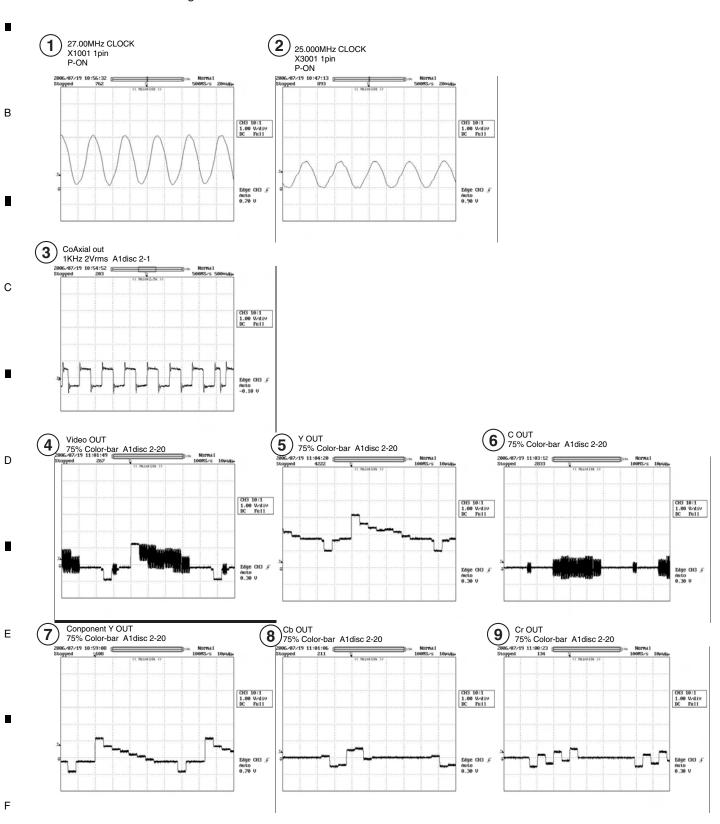
BDP-HD1

3.16 WAVEFORMS

MAIN ASSY

Note: The numbers for the waveform photos (circled) are identical to those for the schematic diagrams, PCB diagrams, and troubleshooting flowcharts.

3



44

,

BDP-HD1

В

С

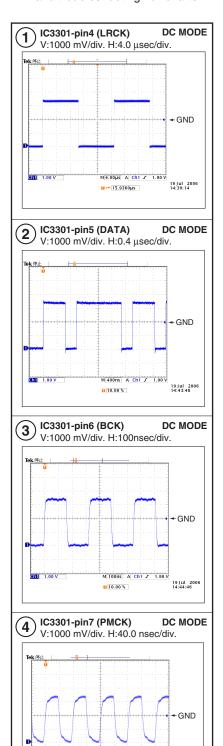
D

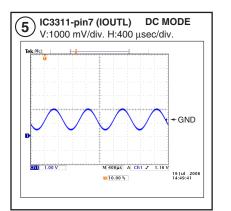
Ε

8

Note: The numbers for the waveform photos (circled) are identical to those for the schematic diagrams, PCB diagrams, and troubleshooting flowcharts.

6





RDL-HD1

45

_

M 40.0ns A Ch1 J 1.90 V

10.00%

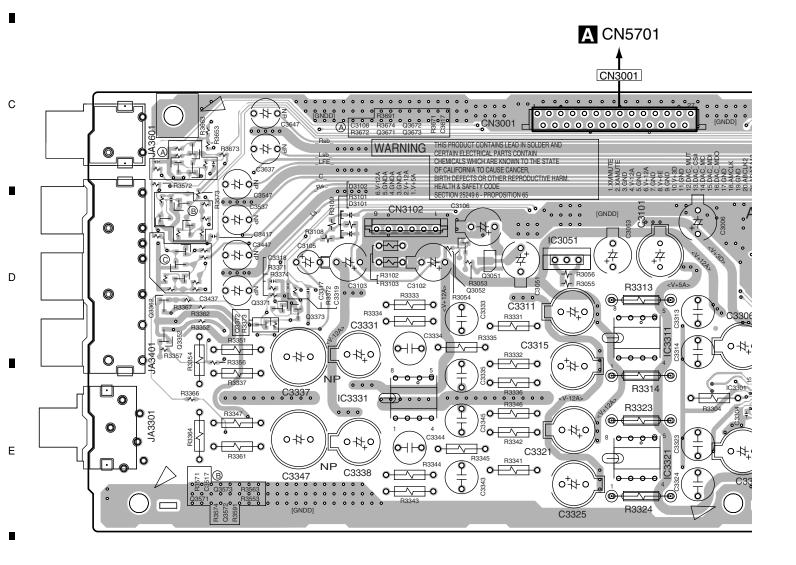
5

19 Jul 2006 14:45:57

4. PCB CONNECTION DIAGRAM 4.1 AUJB ASSY

SIDE A

D AUJB ASSY



Q3362 Q3352 Q3371 Q3373 Q3671 Q3672 Q3051 IC3051 IC3311 IC3301
Q3372 IC3331 Q3673 Q3052 IC3321
Q3573

Q3571 Q3572

BDP-HD1

SIDE A

В

D

Ε

8

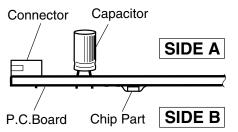
NOTE FOR PCB DIAGRAMS:

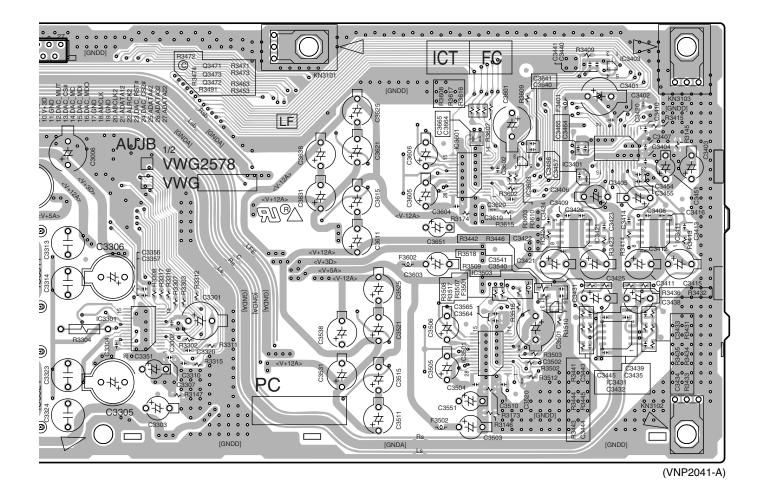
- 1. Part numbers in PCB diagrams match those in the schematic
- 2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name	
000 B C E	B C E B C E	Transistor	
• <u>000</u> B C E	B C E B C E	Transistor with resistor	
000 DGS		Field effect transistor	
@00\\\	******	Resistor array	
000		3-terminal regulator	

- 3. The parts mounted on this PCB include all necessary parts for several destinations.
- For further information for respective destinations, be sure to check with the schematic diagram.

 4. View point of PCB diagrams.





IC3401 IC3403 IC3411 IC3421 IC3431

IC3601

IC3501

IC3503

IC3603

8

311

321

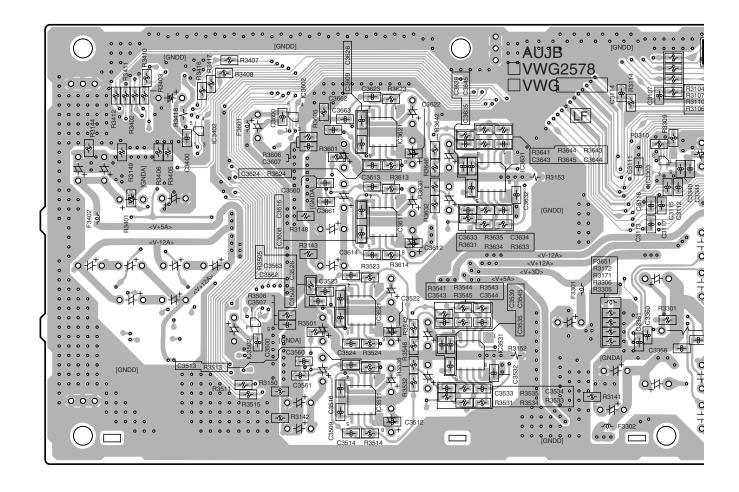
IC3301

Q3471

Q3473

Q3472

D AUJB ASSY



IC3402 IC3502 IC3602 IC3621 IC3631 IC3303
IC3611 IC3531
IC3521
IC3511

D

-

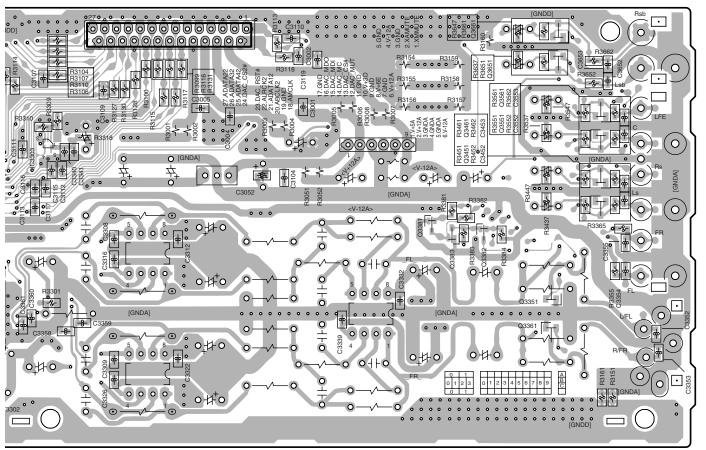
ו טח-חטו

В

D

Е

CN3001

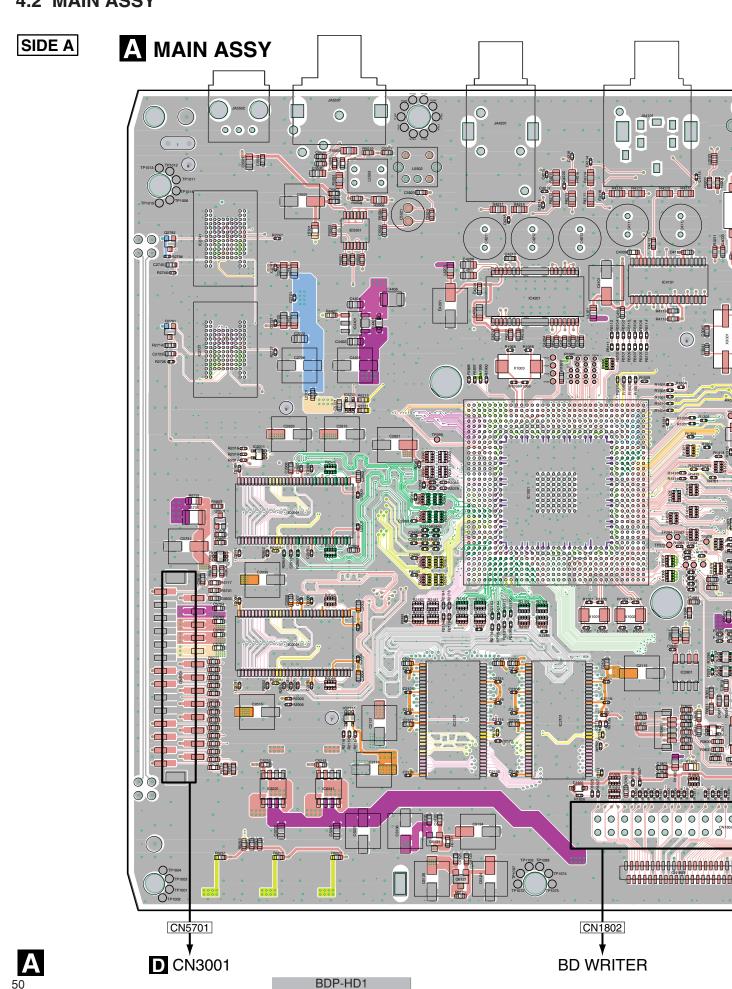


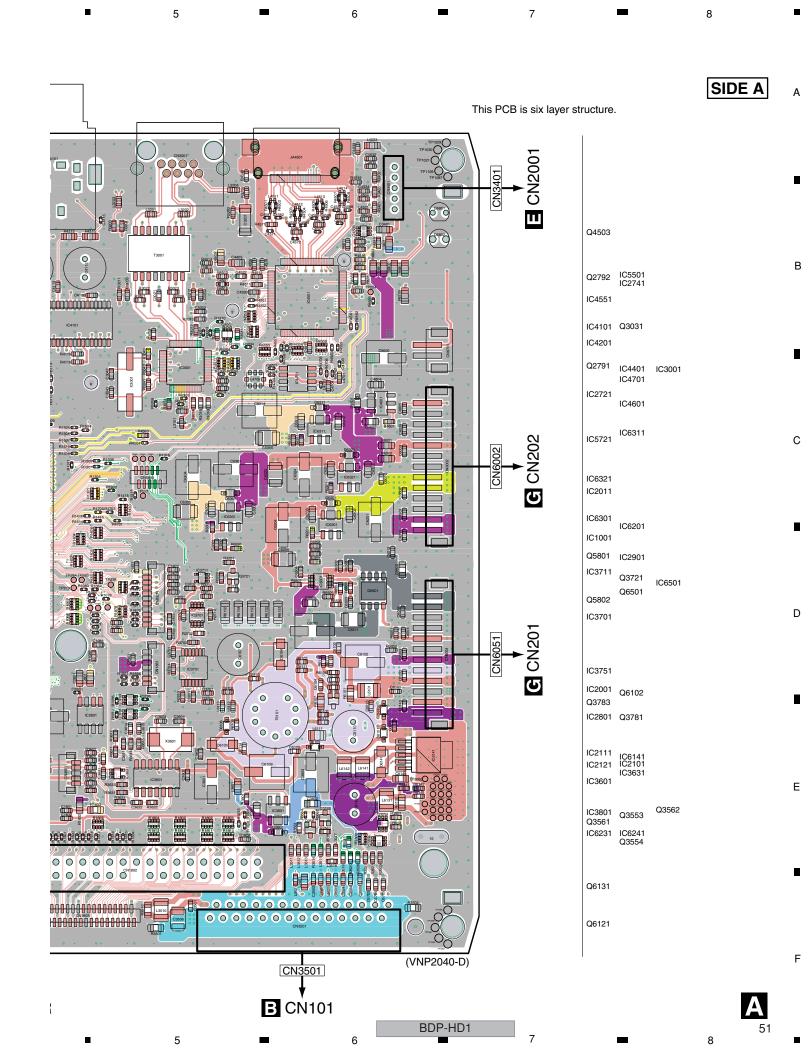
(VNP2041-A)

8

IC3303 Q3381 Q3661 Q3461

Q3383 Q3551 Q3351 Q3382 Q3361





A MAIN ASSY

IC4611 IC3903 IC3902 IC3901 IC6211 IC6221 IC6251

Q4582 Q4581 Q4591 Q6706 Q6701

Q6705

Q4201

Q4221

Q4231

Q4121

Q4131

Q4141

IC2921

Q6101

Q3784 IC2021

IC3921

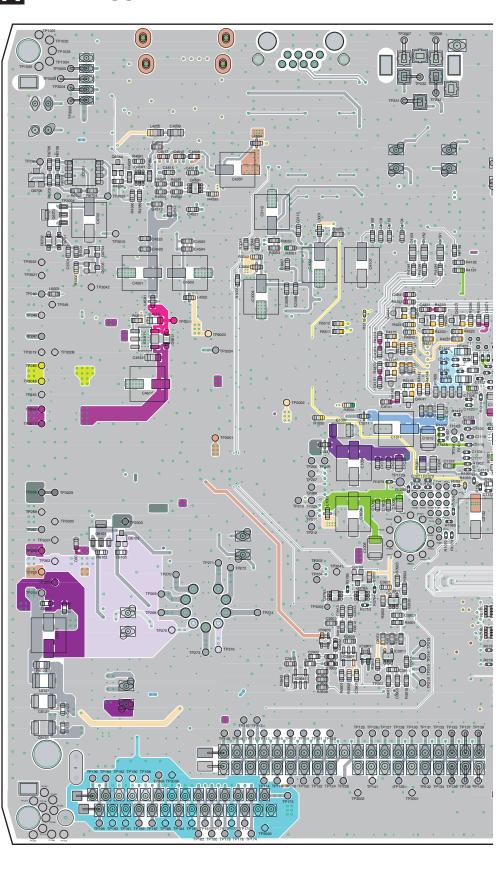
IC3641

Q6103

Q3782 Q3785

IC3911

Q6704 IC2761 IC2701





D

BDP-HD1

В

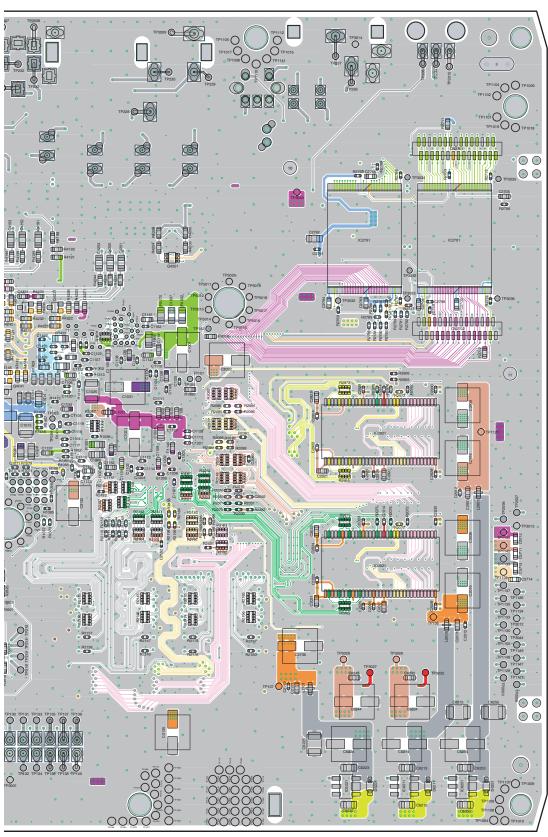
С

D

Ε

8

This PCB is six layer structure.



6

5

5

(VNP2040-D)

A

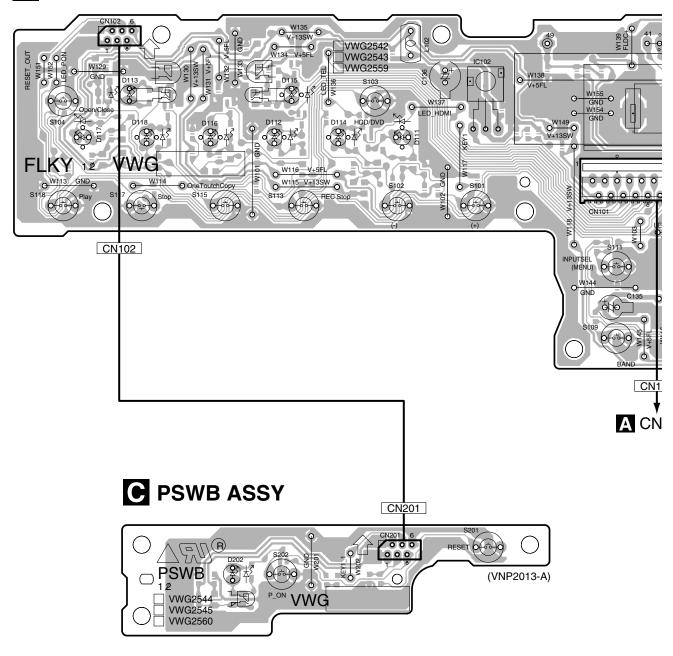
8

BDP-HD1 7

4.3 FLKY and PSWB ASSYS

SIDE A

B FLKY ASSY



B C

BDP-HD1

SIDE A

8

IC102

W112 V+5FL J101

(VNP2013-A)

В

D

Е

В

6

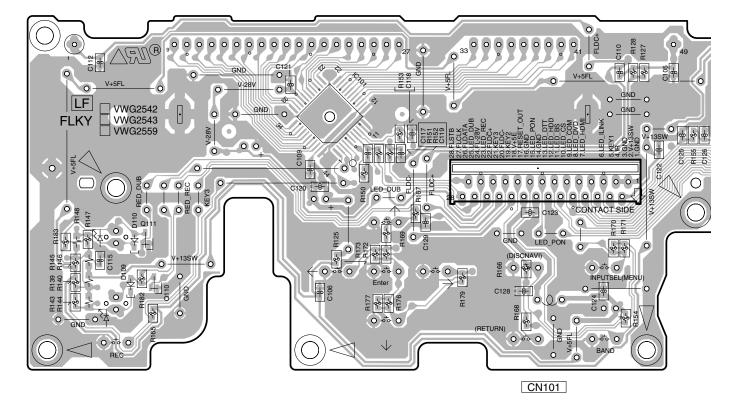
0

5

CN101

A CN3501

B FLKY ASSY



B

BDP-HD1

5 6 7 8

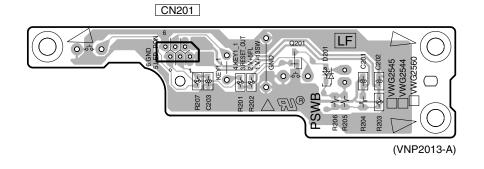
SIDE B

В

CN102

| CN102 | CN102 | CN103 | CN103

C PSWB ASSY



ВС

Е

6

4.4 SRJB and WRPB ASSYS

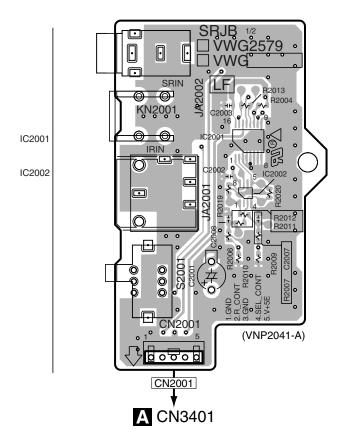
SIDE A

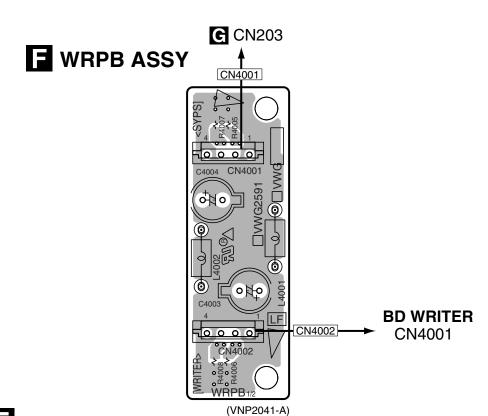
В

D

Е

E SRJB ASSY



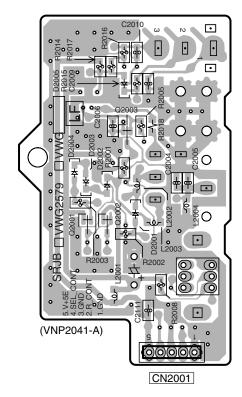


BDP-HD1

В

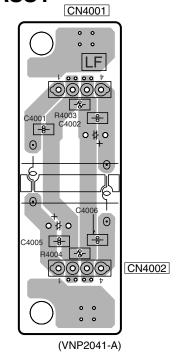
E SRJB ASSY

5



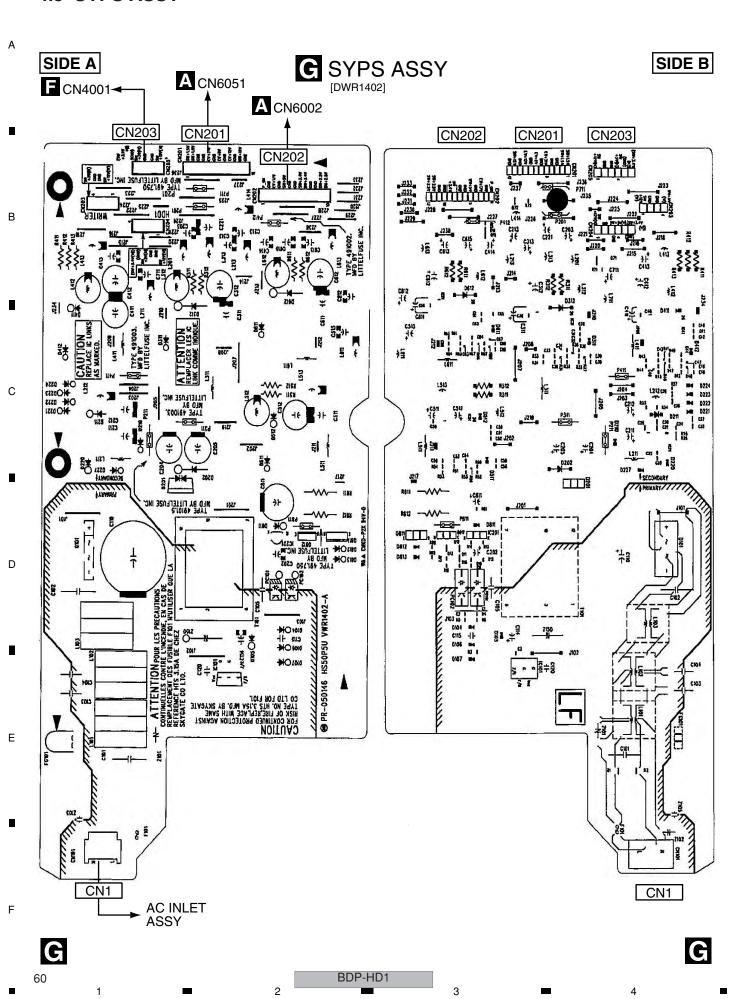
Q2003 Q2002 Q2001

WRPB ASSY



BDP-HD1

Е



- The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- When ordering resistors, first convert resistance values into code form as shown in the following examples. Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

 $5.62k \Omega \rightarrow 562 \times 10^{1} \rightarrow 5621 \dots RN1/4PC \boxed{5} \boxed{6} \boxed{2} \boxed{1} F$

Mark No.	Description	Part No.	Mark No.	Description	Part No.
LIST OF ASS	•		Q3721,3784,		DTC124EUA
		VVV01E1	Q3781–3783		UMH9N
1MAIN A	4551	VXX3151	Q4121,4131,	·	2SA1576A
NSP 1FLKB	100V	VWM2357	Q4231,4241,	4582,6102	2SA1576A
2FLKY		VWWG2559			
	B ASSY	VWG2559 VWG2560	Q4503		UM6K1N
21 344	D A001	VVVG2300	Q4581		HN1C03FU
NSP 1AUSR	ACCV	VWM2394	Q4591		UMD2N
2AUJB		VWWG2578	Q6101		2SC5712
2SRJE		VWG2578 VWG2579	Q6103		2SC4081
	B ASSY	VWG2573 VWG2591	00101		0000070
2	D AGO I	V V G 2 3 3 1	Q6121		2SD2673
1SYPS	ASSY	VWR1402	Q6131 Q6501 MOS	CCT	2SA1036K
<u></u> 1011 0 1	1001	V VVIII +02	D3902		RTW060N03
					RB520S-30
			D4601		RB501V-40
<u>Mark No.</u>	Description	Part No.	D6101		UDZS15(B)
			D6102		1SS355
A MAINI	4 O O V		D6102		UDZS13(B)
A MAIN			D6104,6105,	6141	RF101L2S
<u>SEMICONDU</u>	<u>CTORS</u>		D6106	0111	UDZS2R4(B)
IC1001		SMP8634LF-A	20100		00202111(0)
IC2001,2021,2	2901,2921	K4H510838C-UCCC	MISCELLAN	IFOLIS	
IC2101,2121		K4H511638C-UCCC	L1001,1011,		DTL1106
IC2701		VYW2378	L2001,1011,		DTL1106
IC2801		BR24L01AFJ-W	L2801,3401,3	-	CTF1394
			L3001,3002,	·	DTL1106
IC3001 LAN I	C	RTL8201CP-LF	L3201–3204	-	VTH1056
IC3601		PE0003C	20201 0204	OOIL	V 1111000
IC3631,3711,3	3911,3921	TC7SH08FUS1	L3510,5731,6	6101.6141	VTL1175
IC3701		TC7WH74FU	L3511–3513.	·	CTF1306
IC3751,5501		TC74VHCU04FT	L3521,3523,		CTF1306
A			L3635,3701,4	·	CTF1357
⚠ IC3801 REGU	JLATOR IC	S-1170B50UC-OUJ	L4101,4201,4	·	CTF1394
IC3901		BD45282G	, ,	,	
IC3902		BU4809F	L4502,4504	EMI FILTER	DTL1106
IC4101	550 445	LA73054	L4511-4514	COIL	ATH7022
IC4201 HD VI	DEO AMP	SM5302AS	L4532,4534,6	6003	CTF1306
104404		C 1170DE0LIC OLII	L4533,5501	INDUCTOR	CTF1394
⚠ IC4401	TDANICMITED	S-1170B52UC-OUL	L5502 COIL		VTL1172
	TRANSMITER	SII9030CTU-7			
		NJM2880U1-05 S-1170B18UC-OTD	L5503 COIL		PTL1017
IC4701		ICS571MLF	L5706 INDU		CTF1384
104701		10007 TIVILI	L6111 CHIP		BTH1119
IC5721		TC7SZ08FU	L6113 INDU		CTF1357
/!\ IC6141		PQ1CZ41H2ZPH	F5504 CHIP	MAGNET CORE	DTF1068
⚠ IC6201,6211,6	3221 6251	S-1170B26UC-OTL		DE 100	D.T
/!\ IC6301,6311,6		S-1170B33UC-OTS	F5505 CHIP		DTF1070
∴ IC6501,5511,6 ∴ IC6501	· ·	BD3504FVM		MB. JACK (S+1P)	AKB7159
		25000 II VIVI	JA4201 3P F		VKB1198
Q3031,3553,3	554.4201	UM6K1N		MI CONNECTOR	AKP1278
	,		JA5501 1P F	21ΝΙΔ(:K	AKB7102

BDP-HD1

7

Ε

В

	·	-	-	•
	Mark No. Descrip	otion Part No.	Mark No. Description	Part No.
			R2170-2172,2178	RS1/16SS100J
	JA5502 OPT. LINK OUT	VKS1002	R2174,2945,2955,2965	RAB4CQ220J
Α	T3001 10/100BASE-T TRAI			
	T6101 TRANSFORMER	VTT1166	R2181–2183,2187,2941	RAB4CQ100J
	X1001 (27MHz) CRYSTAL	VSS1205	R2184–2186,2188,2189	RS1/16SS100J
	X3001 (25MHz) CRYSTAL	VSS1215	R2381–2383,2393,2481	RS1/16SS0R0J
	CN1802 40P ATA CONNEC	CTOR VKN2059	R2483,2491,2493,2703 R2706,2715–2717,2781	RS1/16SS0R0J RS1/16SS0R0J
	CN1861 7P CONNECTOR	VKN1411	H2700,2713—2717,2781	N31/10330N00
	CN1871 11P CONNECTOR		R2791,2799,4551,4552	RS1/16SS0R0J
	CN3001 RJ45 CONNECTO		R2794,3033,3034	RS1/16SS103J
	CN3401 5P PLUG	KM200TA5	R2905,2906	RS1/16SS1001F
			R2948,2961,2968	RAB4CQ100J
	CN3501 28P CONNECTOR	52044-2845	R2950-2952,2970-2972	RS1/16SS100J
	CN3601 5P CONNECTOR	VKN1374		
В	CN5701 CONNECTOR	VKN2011	R2958,2975,2976,4564	RS1/16SS220J
	CN6002 PH 13P CONNEC		R2973,3011	RAB4CQ220J
	CN6051 PH 12P CONNEC	TOR AKM1283	R3012,3013	RS1/16S1001F
			R3021–3024	RS1/16S49R9F
	<u>RESISTORS</u>		R3201-3204,4121,4122	RS1/16S75R0F
	R1001,1002,1031,1069	RS1/10S0R0J	D0500	DAD4CO100 I
	R1051,1053,1059,1836	RS1/16SS0R0J	R3503 R3781–3786.3788	RAB4CQ102J RS1/16SS332J
_	R1052,1054	RS1/16SS105J	R4111–4113,4211–4213	RS1/10S75R0F
	R1056,1401–1404,1406	RAB4CQ330J	R4111–4116,4211–4216	RS1/10S0R0J
	R1057,1058,1061–1064	RS1/16SS330J	R4131,4132,4141,4142	RS1/16S75R0F
	R1065,1068,1074,1076	RS1/16SS103J	114101,4102,4141,4142	1101/100/01101
	R1066,1067,1878,1879	RAB4CQ103J	R4221,4222,4231,4232	RS1/16S75R0F
С	R1070,1833,3501,3502	RS1/10S0R0J	R4241,4242	RS1/16S75R0F
O	R1071,1075,2050–2052	RS1/16SS100J	R4553-4556,4559	RAB4CQ0R0J
	R1072,1073,1081–1084	RS1/16SS330J	R4557,4558,4560,4565	RS1/16SS0R0J
			R4561,4562	RS1/16SS4700F
	R1077,1085-1087,1315	RS1/16SS103J		
	R1301,2045,2055,2065	RAB4CQ220J	R4705	RN1/16SSE1000D
	R1302-1314,1501-1510	RS1/16SS220J	R4708	RS1/16SS470J
-	R1407,1409,1412,1419	RS1/16SS103J	R5101,5103,5105,5107	RS1/16SS0R0J
	R1410,1810–1813,1824	RAB4CQ330J	R5109,5111,5113,5115	RS1/16SS0R0J
			R5506	RS1/10S75R0F
	R1413–1416,1808,1823	RS1/16SS330J	R6001,6002,6123,6133	DC1/10C0D0 I
	R1421,1422	RN1/10SE1300D	R6001,6002,6123,6133	RS1/10S0R0J RS1/10S221J
D	R1801–1806	RAB4CQ223J	R6151–6155	RS1/4SA472J
D	R1807,1831 R1814,1818,1821	RS1/16SS223J RS1/16SS820J	R6505	RS1/16S3301F
	R1014,1010,1021	HS1/1655620J	R6506	RS1/16S3901F
	R1815	RS1/16SS562J	RESISTORS	1101/1000011
	R1816,1817,1820,2057	RS1/16SS220J	Other Resistors	RS1/16S###J
	R1819	RS1/16SS102J	Ctrior registers	1101/100////10
_	R1822,1826,1861,1862	RS1/16SS103J	CAPACITORS	
	R1830,1864,1865	RS1/16SS330J	C1001,1004,1011,1021	CEVLW221M4
	, , - 		C1001,1004,1011,1021 C1002,1012,1022,1032	CKSRYF105Z10
	R1871-1876,4701	RS1/16SS330J	C1003,1013,1023,1033	CCSRCH102J50
	R1877,1892–1894,2786	RS1/16SS103J	C1005–1007,1014,1024	CKSQYB106K6R3
	R1891,1895	RAB4CQ103J	C1008,1037 (150 uF/ 4 V)	VCH1266
	R1898,1900,1901,1903	RS1/16SS0R0J	, , , ,	
Е	R2005,2006,2105,2106	RS1/16SS1001F	C1031,1034,2016,2036	CEVLW221M4
			C1035,1036,2702,2801	CKSQYB106K6R3
	R2019,2078,2084–2086	RS1/16SS0R0J	C1051	CCSSCH120J50
	R2041,2048,2061,2068	RAB4CQ100J	C1052	CCSSCH100D50
	R2058,2075,2076,2140	RS1/16SS220J	C1101–1112,1151,1153	VCG1063
	R2070–2072,2143,2144	RS1/16SS100J	• • • • • • • • • • • • • • • • • • • •	01/603/2010
	R2073,2145,2146,2155	RAB4CQ220J	C1113–1128,1201,1203	CKSSYF104Z16
	R2081–2083,2087	RAB4CQ0R0J	C1129–1141,1152,1154	CKSRYF105Z10
	R2088,2089,2119	RS1/16SS0R0J	C1161,1428,1801,1802	CKSRYF105Z10
	R2141,2142,2148,2149	RAB4CQ100J	C1162,1202,1205,1425	VCG1063
	R2147,2142,2140,2149	RS1/16SS220J	C1204,1206,1421,1422	CKSSYF104Z16
	R2150–2152,2163,2164	RS1/16SS100J	C1423,1424	CKSSYB822K16
F			C1423,1424 C1426,1427,2003	CKSSYF104Z16
	R2156,2165,2166,2173	RAB4CQ220J	C1420,1427,2003 C1821	CCSRCH470J50
	R2161,2162,2168,2169	RAB4CQ100J	C1861,1871,2001,2002	CKSRYF105Z10
	R2167,2175,2176,2957	RS1/16SS220J	C2004,2008,2021,2023	CKSRYF105Z10
	62	BD	P-HD1	
	1 1	2	3	4

	5	6		7	8	
ark No.	Description	Part No.	Mark No.	Description	Part No.	
C2005,2006,2	2024.2025	CKSSYB103K16	C6005.6011-	6016.6105	CKSRYB103K50	
C2007,2009,		VCG1063	C6101,6103,6		CKSRYF104Z50	
C2011-2014	,2022,2030	CKSSYF104Z16	C6102 (68 ul	F/16 V)	VCH1267	
C2015,2115,		VCH1234	C6104,6503,6		CKSRYB223K50	
C2027,2101,	2102,2104	CKSRYF105Z10	C6107,6110,6		CEHAZA101M35	
C2028,2029,2	-	VCG1063	C6109		CEVW100M50	
C2035,2116,2	· ·	CEVW221M4	C6122,6123,6	· ·	CKSRYF104Z50	
C2103,2111-	·	CKSSYF104Z16	C6126,6134,6		CEVW101M16	
C2105,2106,	-	CKSSYB103K16	C6133,6135,6		CKSRYF104Z50	
C2108,2121,	2123,2127	CKSRYF105Z10	C6203,6213,6	0223,6253	CKSQYB106K6R3	
C2110,2126,	-	VCG1063	C6205	2202 6212	VCH1258	
C2130,2701,2 C2135,2136,2	· ·	CKSSYF104Z16 CEVLW221M4	C6222,6252,6 C6301	0302,0312	CKSQYB225K10 CEVW101M16	
C2135,2136, <i>i</i> C2703,2704, <i>i</i>	-	CKSRYF105Z10	C6303.6313.6	2222 6502	CKSQYB106K6R3	
C2705,2704,	,	CKSRYB102K50		6501 (150 uF/4 V)	VCH1234	
52705,5911,	3922	ONSHTB102N30	00314,0324,0	5501 (150 til /4 V)	VOI11254	
C2904,2908,	-	CKSRYF105Z10	C6322		CKSQYB225K10	
C2905,2906,2 C2907,2909,2	· ·	CKSSYB103K16 VCG1063	C6505		CKSQYB106K6R3	
C2907,2909,1 C2911–2914.	-	CKSSYF104Z16				
C2911–2914; C2927,3007,	, , , , , , , , , , , , , , , , , , ,	CKSSYF104Z16 CKSRYF105Z10				
C2020 2020	4705	VCG1062				
C2928,2929,4 C3001,3004,4		VCG1063 CEVLW221M4	D AUJB	ΔSSV		
C3001,3004,4	· ·	CCSRCH102J50				
C3002,3003, C3021,3022,	· ·	CKSRYF104Z50	SEMICONDL	<u>JCTORS</u>		
53021,3022, C3041	3111,3113	CCSRCH200J50	<u></u> IC3051		NJM78M05FA	
03041		CC3HCI 1200030	IC3301,3401,		PCM1738EG-3	
C3042		CCSRCH150J50	IC3311,3321,		OPA2134PAS1	
3042 3044,3507,4	4502	CCSRCH102J50	IC3402,3502		TC7SH08FUS1	
33044,3307, C3112	-30L	CEVLW330M25	IC3411,3421,	3431,3511	NJM5532MD	
	AMIC CAPACITOR	ACG1127				
C3202,3203,		CKSRYF104Z50	IC3521,3531		NJM5532MD	
,0202,0200,	0001 0000	01.01111 10.1200	Q3351,3352,		2SD2114K	
C3401,3802,4	4151–4153	CKSQYB106K6R3	Q3371,3373,	-	2SK2034	
C3402,3611,		CCSRCH101J50	Q3372,3382,0	-	2SA1576A	
C3601,3803,	· ·	CEVW101M16	Q3451,3461,3	3331,3361	2SD2114K	
C3602,3608,	· ·	CKSRYF104Z50	Q3471,3473,	0571 0570	2SK2034	
C3614,3615,		CCSRCH220J50	D3001	33/1,33/3	RB501V-40	
			D3101,3102		1SS355	
C3702,3751,	3901,3912	CKSRYF105Z10	D0101,0102		100000	
C3761,5701-	-5704	CKSRYB104K50				
C3801,4402,	4602,4604	CKSQYB225K10	COILS AND	FII TERS		
C3905,3903		CCSRCH101J50	F3301,3302,3		DTE1070	
C3921,4121,4	4131,4141	CKSRYF105Z10	F3501,3502,3	•	DTF1070 DTF1070	
C4104-4106	·	CKSRYF104Z50				
C4107,4611,		CEVLW470M16	CAPACITOR	9		
C4111,4112,		CEAT102M6R3	C3001,3002,3		CKSRYF104Z25	
C4113,4203-	•	CKSRYF104Z50	C3001,3002,3		CEHAZA471M6R3	
C4202,4207,	4208	CKSQYB106K6R3	C3006,3053,3 C3051,3102,3		CEHAZA471M6R3 CEHAZA221M16	
04040 45	4504 5500	01/05/546 : 356	C3051,3102,3 C3052,3307,3		CEHAZA221M16 CKSRYF104Z25	
C4210,4511-	,	CKSRYF104Z50	C3052,3307,3	0010,0012	CEHAZA102M6R3	
C4221,4231,4	· ·	CKSRYF105Z10	U3101		OLI IAZA IUZIVIONS	
C4251-4253		CKSQYB106K6R3	C3105,3303,3	3403 3405	VCH1249	
C4401,4605,	-	CEVW101M16	C3110,3119,3	•	CCSRCH102J50	
C4504–4506	,4508,4510	CCSRCH102J50	C3302,3341,3	•	CKSRYF105Z10	
C4E07 604 4 4	6004 6054	CEVI M/004 M/4	C3305,3306	,	VCH1261	
C4507,6214,0	-	CEVLW221M4	C3308,3309,3	3327.3408	CCSRCH331J50	
C4509,4613, C4522,4523,	· ·	CKSQYB106K6R3 CCSRCH102J50	30000,0000,0	,		
	· ·	CKSQYB225K10	C3311,3315,3	3321,3325	VCH1257	
C4612,6144,0 C4703	0202,0212	CKSQYB225K10 CKSSYF104Z16	C3313,3314,3	•	VCE1051	
04700		UNSS 1 F 1042 10	C3316,3322,3	•	CKSRYF104Z25	
C5501,6204		CEVW221M4	C3331,3338		VCH1257	
C5501,6204 C5502,5525,	5528 5721	CKSRYF105Z10	C3333,3343		VCE1052	
C5502,5525, C5521 (47 u	· ·	VCH1241	33300,00-40			
C6001–6003	,	CKSRYF105Z10	C3334,3335,3	3344,3345	VCE1051	
C6001-6003	· · · · ·	CKSRYF105Z10 CKSRYF104Z50	C3337,3347	· · · · · · · · · · · · · · · · · ·	VCH1255	
JUUU+,UUJ I,I	000 <u>2,</u> 000 4	ONOTH 104230	BDP-HD1		- -	63
	5	6	וטוו- וטט	7 -	8	US
		-				

ark <u>No.</u>	Description	Part No.	Mark No. Description	Part No.
C3351,3451,35	51	CCH1510		
C3401,3501		VCH1248		
C3406,3503,35	05,3506	VCH1249	COILS AND FILTERS	
C3407,3410,34	10 2/16	CKSRYF104Z25	L2002–2005	CTF1394
C3409,3427,35		CCSRCH331J50	F2001	DTF1070
	•	VCH1247		
C3411,3415,34	•	CCSRCH471J50	OW/# OUT O 1115 1115	
C3413,3414,34 C3422,3426,35		CKSRYF104Z25	SWITCHES AND RELAYS	
00422,0420,33	00,0001	ONORTH 104220	S2001	VSH1009
C3431,3438,35	11,3515	VCH1247	CARACITORS	
C3433,3443,35	,	CCSRCH122J50	CAPACITORS	OE 4T404144
C3434,3435,34	,	CCSRCH471J50	C2001	CEAT101M16
C3437,3447,35	•	CEANP470M16	C2002,2003,2005,2009	CKSRYF104Z25
C3502,3541		CKSRYF105Z10	C2004,2006	CCSRCH471J50
			C2007,2008	CKSRYB153K25
C3510,3512,35	16,3522	CKSRYF104Z25	C2010	CCSRCH681J25
C3513,3514,35		CCSRCH471J50	00446	01/05//545 :305
C3521,3525,35	•	VCH1247	C2111	CKSRYF104Z25
C3526		CKSRYF104Z25		
C3527		CCSRCH331J50	BE010F3-3	
			<u>RESISTORS</u>	
C3534,3535,35	44,3545	CCSRCH471J50	All Resistors	RS1/16S###J
C3540	•	CCSRCH102J50		
			OTHERS	
			<u>OTHERS</u>	
<u>ESISTORS</u>			JA2001 H.P JACK	RKN1006
R3001-3008,30	•	RS1/10S0R0J	JA2002 REMOTO JACK	RKN1004
R3108,3109,33	18,3418	RS1/10S0R0J	KN2001 TERMINAL	VNE1948
R3304		VCN1141	CN2001 5P SOCKET	KP200TA5L
R3313,3314,33	23,3324	VCN1140		
R3331-3333,33	336	VCN1138	_	
Door to see a see	44.0045	VON4465	WRPB ASSY	
R3334,3335,33	44,3345	VCN1139		
R3337,3347		VCN1136	COILS AND FILTERS	
R3341–3343,33		VCN1138	L4001,4002	VTH1013
R3351,3354,33	61,3364	VCN1137		
R3401,3501		RN1/16SE1602D	<u>CAPACITORS</u>	
De 4/5 5 11 1		BN1/// 60=	C4001,4002,4005,4006	CKSRYB105K16
R3413,3414,34	•	RN1/16SE6200D	C4003	CEAT100M50
R3431–3433,34		RN1/16SE1201D	C4004	CEHAZA221M16
R3434,3435,34		RN1/16SE1801D		
R3441–3443,34		RN1/16SE1201D	<u>OTHERS</u>	
R3513,3514,35	23,3524	RN1/16SE6200D	CN4001,4002 4P TOP POST	B4B-EH
R3518		RS1/10S0R0J		
R3531–3533,35	536	RN1/16SE1201D		
R3534,3535,35		RN1/16SE1801D	C PSWB ASSY	
R3541–3543,35	•	RN1/16SE1201D		
Other Resistors		RS1/16S###J	<u>SEMICONDUCTORS</u>	
Out 1 100101010		1 (Ο 1/ 1 Ο Ο π ππο	Q201	DTC124EUA
			D202 LED(BLUE)	SLR-343BBT(GHJk
THERS			MICORI : 11170117	
JA3301 2P PI	N JACK	AKB7104	MISCELLANEOUS	
JA3401 6P PI		VKB1235	CN201 6P FFC CONNECTOR	VKN1237
KN3101–3103		VNF1084	S202 TAKT SWITCH	VSG1024
			DEGIOTORO	
CN3001 B TO	B CONNECOR	VKN2008	RESISTORS	B0
			All Resistors	RS1/16S###J
			CARACITORS	
-			CAPACITORS C201, 202	CKCDVE10470F
SRJB A	SSY		0201, 202	CKSRYF104Z25
EMICONDUC	IORS	TOT 1110 :		
IC2001		TC74HC4053AFT	B FLKY ASSY	
IC2002		TC7WH34FU		
Q2001,2002		DTA124EUA	<u>SEMICONDUCTORS</u>	
Q2003		DTC124EUA	IC101 FL	PT6315
D2001-2004		1SS355	Q101–103,105, 107	DTC124EUA
		DDE041/ /2	D113, 115	SLR-343BBT (GHJ)
		RB501V-40	D111, 112, 116, 118	SLR-343VC (NPQ)
D2005				
D2005		BDP	-HD1	

В

С

D

Ε

F

5 **-** 6 **-** 7 **-** 8

Α

В

С

D

Ε

65

Mark No. Description Part No.

MISCELLANEOUS

 S101-118 TAKT SWITCH
 VSG1024

 CN101 28P FFC CONNECTOR
 52492-2820

 CN102 6P FFC CONNECTOR
 VKN1237

 V101 FL TUBE
 VAW1084

 IC102 REMOTE RECEIVERE UNIT
 RPM7140

100 FL HOLDER VNF1130

RESISTORS

All Resistors RS1/16S###J

CAPACITORS

C109, 123

C136 CEJQ101M16
C135 CEJQ101M6R3
C105, 112, 127- 129 CKSRYB103K50
C122 CKSRYB105K16
C104, 107, 113, 120, 121, 124 CKSRYF104Z25
C130, 131, 132 CKSRYF104Z25

CKSRYF105Z10

SYPS ASSY [VWR1402]

5

SYPS assembly has no service part.

BDP-HD1 7

When Adju

■ Exchange Parts of Mechanism Assy

Exchange the DRIVE ASSY

В

С

D

Е

•

Adjustment Points

3

Mechanical • None point

• ID NUMBER and DATA SETTING
• FIRMWARE UPDATE

■ Exchange PCB Assy

Exchange MAIN ASSY



Mechanical point • None

BDP-HD1

• ID NUMBER and DATA SETTING
• FIRMWARE UPDATE

1 = 2

[Purposes]

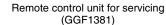
• An individual ID number and ID data (AACS, CPRM, BD+, Windows Media DRM, and MAC address) must be input at the same time. All data are determined according to the data on the ID data disc. If the number and data are not set correctly with the following procedure, the unit does not work properly. You will find the ID number to be labeled on the rear panel.

This setting is Necessary When:

• When the DRIVE Assy or MAIN Assy is replaced.

[Tools to be used]







ID Disc for Blu-ray Player (GGV1306)

[Notes]

Important: If no ID label is found on the rear panel, write down the specified ID number by checking it on the version check screen ([ESC] + [DISP]).

- Input the ID number while the unit is in Stop mode.
- After the data are read from the ID data disc, the disc will automatically be unloaded.
- Each time a key input succeeds, the screen background becomes blue. If a key input fails, the screen background becomes red.

5

В

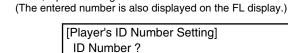
Ε

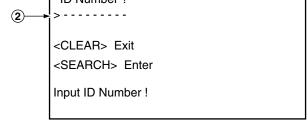
How to Input the ID Number and ID Data

① To enter the input mode, press ESC+STEREO keys sequentially in a status with no ID number set, such as after FLASH-ROM downloading. ■



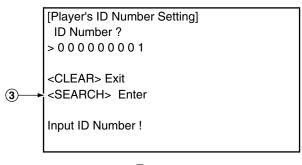
(2) As number input is enabled when the unit enters the input mode, input the 9-digit ID number.







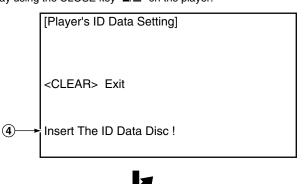
(3) After inputting the number, press SEARCH keys to register the ID number. (SEARCH key is not accepted until 9 digits are entered.)



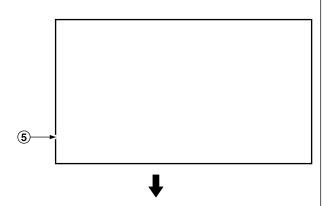


When the ID number has been registered, the unit enters the ID data input mode.

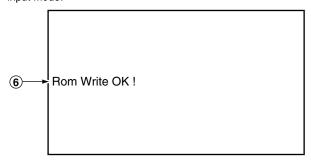
In this condition, place the ID data disc on the tray and close the tray using the CLOSE key "■/▲" on the player.



(5) While the data are being read, no indication is displayed (black screen) .



- (6) When the ID data have been written to the FLASH-ROM, the message "Rom Write OK" is displayed on the screen. (The FL display indicates "ID OK.")
- 7 After confirming this message, press <u>CLEAR</u> key to exit the input mode.



_

Ε

В

С

D

DI

3

[Example of indications on the FL display when a numeric ID number is input]

Order of numeric inputs: 0, 1, then 2

012.....

Note: An ID number is not displayed during the process of clearing the ID number, regardless of whether an ID number has already been registered or not.

If an ID number is already registered, the new ID number will be written over the previous one.

С

В

D

Ε

UPDATE PROCEDURE

В

С

D

Ε

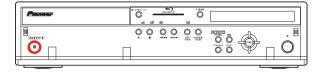
APPLICATION UPDATE

- 1. Plug a power cable into the unit.
- 2. Press the "STANDBY/ON" button to switch the unit on.
- 3. Press the "OPEN/CLOSE" button to open the disctray.
- 4. Place an application UPDATE disc on the tray.
- 5. Press the "OPEN/CLOSE" button on the front panel to begin the application update.
 - * FL display indicates "DL OK" and the unitauto matically switches into standby with the tray opening.

3

* The update time takes 5 to 25 minutes, it changes depending on the version.

DO NOT unplug the power cable or press the standby button until the unit switches into standby mode.



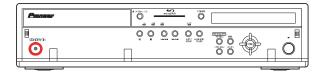
- Remove the application UPDATE disc from the tray.
- Press the "STANDBY/ON" button to switch the unit on, and check if FL display indicates "DL OK". The updato is completed if FL display indicatates "DL OK".

BDP-HD1

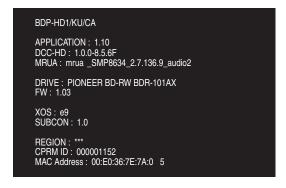
UPDATE PROCEDURE

2) VERSION CHECK

1. Press the "STANDBY/ON" button on the front panel to switch the unit on.



2. Press the "ESC" button and press the "DISP" button on the service remote to display the application version.



- 3. Check if the Application is properly updated to the latest version.
- 4. Press the "ESC" on the service remote to hide the version check screen.

Check with accessory remote controller

- 1. Press the "Home Menu" button
- 2. Select "Initial Setup" and press "Enter"
 3. Select "Audio Out" "Dolby Digital Out "Dolby Digital"(3rd layer)
- 4. Press the "Angle" button



BDP-HD1

6

71

8

8

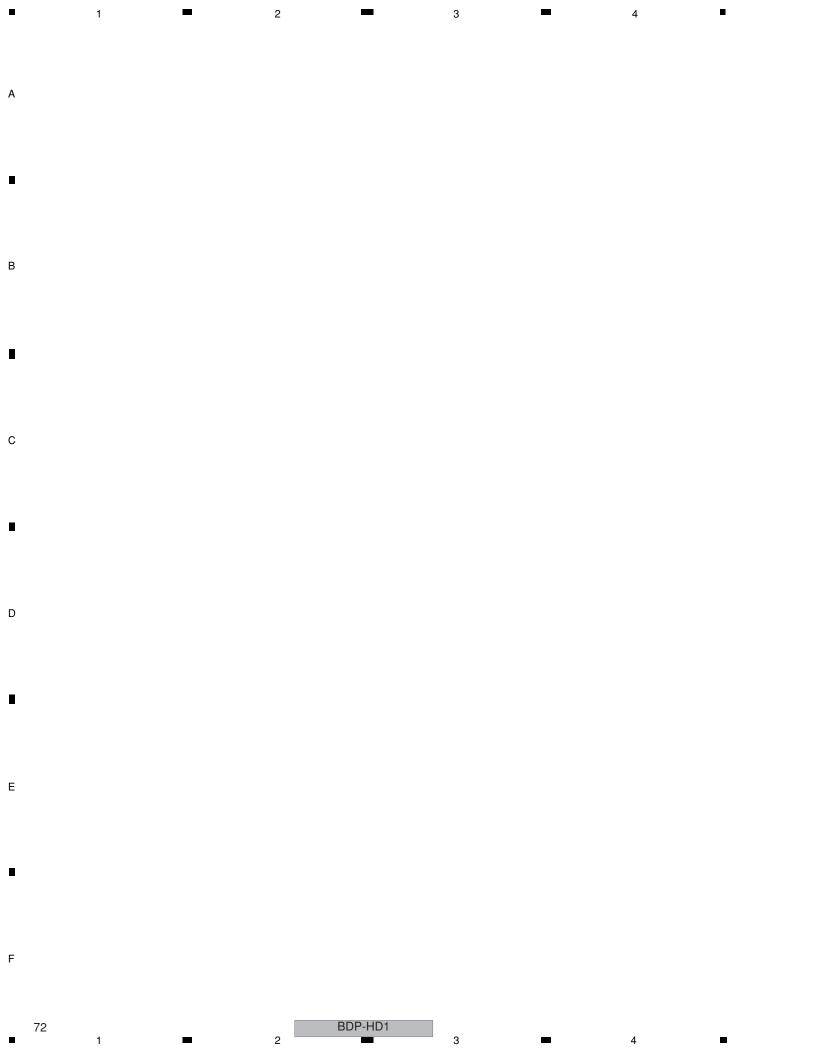
Α

В

С

D

Ε



7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 SERVICE KEY INPUT

How to enter each check mode

- Each check mode described in this specification can be entered even during Normal Operation mode or for CA check, by using the remote control unit for servicing.
- Key names enclosed in quotation marks (" ") are those on the remote control unit for servicing.

No.	Command Name	Key Input	Operation/Usage	Remarks
1	Settings at shipment	Press "ESC" then "CLEAR."	For restoring the settings at shipment (The unit will not be turned off.)	Special condition for entering the mode: The unit must not be in Playback mode. This check mode for settings at shipment (the unit will be turned off) is the same as that entered by simultaneously pressing the STOP and POWER keys on the main unit.
2	Error-Rate Measurement mode 1 (with judgment)	Press "ESC" then "SIDE B."	After automatic error-rate measuring, the results are displayed.	For details, refer to "7.1.3 How to measure the error rate."
3	Search mode	Press "ESC" then "+10."	Switching the numeric-key search from Chapter Search to Title Search during playback of BD-ROM or DVD-Video discs.	
4	Checking of the keys on the main unit	Press "ESC" then "SIDE A."	display. If check results of pressing all the keys on the main unit	Keypresses can be in no particular order. After all the keys on the main unit are pressed, all the segments on the FL display light. Until that, the corresponding key code is displayed when any key is pressed.
		Press "ESC" then "8."	The same operation as that when setting the Component output to 480i.	
5	Switching of the settings	Press "ESC" then "TV/LDP."	The same operation as that when setting the Component output to 480p.	
	for OUTPUT FORMAT	Press "ESC" then "1."	The same operation as that when setting the Component output to 1080i.	The initial setting is Auto.
		Press "ESC" then "CX."	The same operation as that when setting the Component output to 1080p.	
6	Indications for Servicing	Press "ESC" then "DISP."	For details on operations after key inputs, see the sheet "7.1.2 Screen indication for Servicing."	
7	CPRM ID Registration mode	Press "ESC" then "STEREO."	Enter the specific ID number for the recorder, press the CPRM and HDCP (and DTCP) keys, then enter the MAC address.	For details, see "6.2 CPRM ID number and Data setting."
8	Model Identification mode	Press "ESC" then "DIG/ANA."	For confirmation of the destination and version number of the model.	For production use.
9	On-Screen Display output	Press "ESC," "SEARCH," then "6," in that order.	For setting the On-Screen Display output to ON.	Use to stop the On-Screen Display output.
9	On-Screen Display output	Press "ESC," "SEARCH," then "7," in that order.	For setting the On-Screen Display output to OFF.	Ose to stop the On-Screen Display output.
10	Audio muting at the last	Press "ESC" then "9."	For forcibly muting the audio output.	
	stage of output	Press "ESC" then "0."	For forcibly canceling audio muting	
11	Switching of the LED	Press "ESC" then "REPEAT A."	All the segments on the LED display are lit.	
- ' '	display	Press "ESC" then "REPEAT B."	All the segments on the LED display go dark.	
12	Switching of the AUDIO MULTI output	Press "ESC" then "CHAP."	For setting the AUDIO MULTI output to All Channel Output mode	
13	Error-Rate Measurement mode 2 (for continuous playback)	Press "ESC," "DISP," then "2," in that order.	After automatic error-rate measuring, the result is displayed as an OSD.	Special condition for entering the mode: The unit must be in Playback mode. For details, see "7.1.3 How to measure the error rate."
14	4:3 Video out switch	Press "ESC", then "FRM/TIM".	Switch TV ASPECT ratio in Video out to 4:3 (Standard).	The intitial setting is 16 : 9 (Widoscreen).

Specifications of the ESC code

- When the "ESC" key is pressed, ESCAPE mode is entered, and the next keypress will have a special meaning.
- If any key other than the ones indicated in the above table is the first one pressed after the "ESC" key, ESCAPE mode is canceled.
- "ESC" key repeat is ignored, and ESCAPE mode is maintained.

BDP-HD1

73

В

С

D

Ε

Codes to be used in Service mode

Codes for the remote control unit for servicing

2

3

No.	Function	Code
1	ESC	A85F
2	0	A800
3	1	A801
4	2	A802
5	3	A803
6	4	A804
7	5	A805
8	6	A806
9	7	A807
10	8	A808
11	9	A809
12	+10	A81F
13	CLEAR	A845
14	POWER	A81C
15	SIDE A	A84D
16	SIDE B	A84E
17	STEREO	A84A
19	SEARCH	A842
20	DIG/ANA	A80C
21	TEST	A85E
22	DISP	A843
23	CX	A80E
24	REPEAT A	A848
25	REPEAT B	A844
26	CHAP	A840
27	PLAY	A817
28	TV/LDP	A80F
29	FRM / TIM	A841

How to restore the settings at shipment

Make sure that the player's ON

Simultaneously press the STOP and Standby/ON keys on the main unit. The settings at shipment are restored, then the power is turned off.

7/

В

С

D

Ε

BDP-HD1

Α

В

С

D

Ε

1. Specifications of the Version Information screen

• First screen (Version information, etc.)

1 BDP-HD1/KU/CA

5

APPLICATION : 1.00 2

3 DCC-HD : 1, 0, 0 RC33F

(4) MRUA : mrua_SMP8634_2, 7, 136, 34_audio 2

DRIVE : PIONEER BD-RW BDR-101AX

FW: 1.07

XOS : e9 6 SUBCON: 1.3 (7)

REGION

CPRM ID : 000000001

MAC ADDRESS : 00 : E0 : 36 : 00 : C7 :FF

- ① Data on the model: Model name/destination
- 2 Data on the application program: Version for PRA application Note: In the application program, data on DCC-HD, MRUA, built-in drive, SUBCON (PIC,) and XOS are included.
- 3 Data on DCC-HD: Version of middleware for Sigma
- 4 Data on MRUA: Version of the driver for Sigma
- 5 Data on the built-in drive:

Drive name

(5)

8

(9)

(10)

Version

- 6 Data on XOS: Version of firmware for Sigma Chip 8634
- ① Data on SUBCON (PIC):

Version of firmware for the submicrocomputer (PIC)

® Data on regions:

Region numbers for the DVD-ROM. If the region number has not been set, "VIRGIN ROM" is indicated.

- 9 Data on CPRM: CPRM key number If it has not been set, "???????" is indicated.
- 10 MAC address: Value of the MAC address If it has not been set, "????????" is indicated.

BDP-HD1

■ Specifications of error-rate measurement 2 (for continuous playback)

How to start

During playback, press the "ESC", "DISP", then "2" keys, in that order, to measure the error rate continuously and to display the results as an OSD. Those keys are accepted in either Normal Startup mode or Service mode.

Note: For details on key input, see "3. Overview of Screen Change" on the "7.1.2 Screen Indication for Servicing".

Error Rate Measuring

The error rate during playback is measured, and playback time, title and chapter, the address that was read, and the result of measured error rate are displayed as an OSD.

How to measure an error rate

- 1. Press the "ESC", "DISP", then "2" keys, in that order, to start measuring the error rate.
- 2. To cancel and exit Error-Rate Measuring mode, press the "ESC" key while the error rate is being measured.
- While error-rate measuring is stopped, an OSD will remain displayed.

OSD display format

В

D

Ε

(1) TM:**h**m**s	(2) TT:***-**
(3)	(4)
LgcSct	ErrRate
****	*. **E-*
*****	*. **E-*
*****	*. **E-*
*****	*.**E-*
*****	*.**E-*
****	*.**E-*
****	*. **E-*
*****	*.**E-*
****	*. **E-*
****	*. **E-*
****	*. **E-*

(1) Title and chapter data:

Title and chapter numbers for the program being played back

(2) Playback time data:

Elapsed time of the program being played back

(3) LgcSct address data:

Logical sector address where a measurement of error rate starts (Bytes 3 to 6 [information] of the Request Sense Standard Data)

(4) Error-rate data:

Value of a measured error rate

LgcSct address and error rate data will be displayed continuously during playback.

Criterion

Disc Type	Reference Value (less than)
DVD-Video	1.0 x 10 ⁻³
DVD-R	1.0 x 10 ⁻³
DVD-RW	1.0 x 10 ⁻³
BD-ROM	1.0 x 10 ⁻³
BD-R	1.0 x 10 ⁻³
BD-RE	1.0 x 10 ⁻³

BDP-HD1

■ Power On Sequence

The IC3601 then outputs a POWER_ON signal to the SYPS Assy.

After receiving the POWER_ON signal, the SYPS Assy activates, secondary Power, setting it to ON.

The SMP8634 (IC1001), the core LSI, starts up.

Communication between the SMP8634 and the DDR SDRAM starts.

Communication between the SMP8634 and the FLASH_IC starts.

■ Troubleshooting

5

Are the pins at CN6051 and CN6002 supplied with voltages?

 Is the reset signal H? (R1088)

 Is the 27-MHz CLK oscillating? (X1001)

BDP-HD1

77

Α

В

С

D

Ε



7.2 DISASSEMBLY

Note 1: Do NOT look directly into the pickup lens. The laser beam may cause eye injury.

Note 2: Even if the unit shown in the photos and illustrations in this manual may differ from your product, the procedures described here are common.

Note 3: For the performing the diagnosis shown below, the following jigs for service are required.

- GGF1529 : Emergency tray ejection rod.
- GGF1533 : BB Extension board
- GGD1437 : BB Extension cable

Diagnosis of PCB's

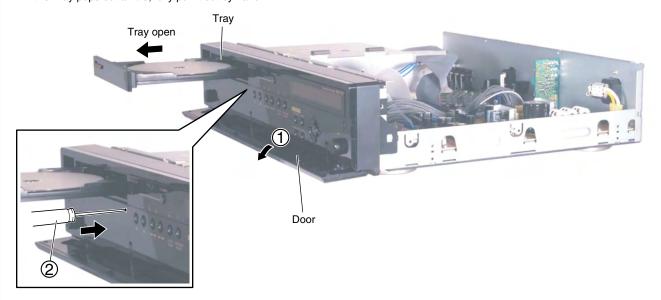
1 Bonnet Case and Tray Panel

- (1) Remove the Bonnet Case by removing the eight screws.
- 2 Press the O STANDBY/ON button to turn on the power.
- 3 Press the OPEN/CLOSE button to open the Tray.
- 4 Remove the Tray Panel.
- (5) Press the O STANDBY/ON button to turn off the power.
- (6) Pull out the Power cord.



How to open the Tray when the power cannot be on

- (1) Open the Door.
- (2) Insert GGF1529 into bore as shown in the following figure. If the Tray pops out a little, fully pull it out by hand.





TIDI

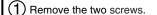
--

Ε

В

1 2 3 4

2 Front Panel Section and Drive ASSY BDR101A



2 Unlock the four hooks.

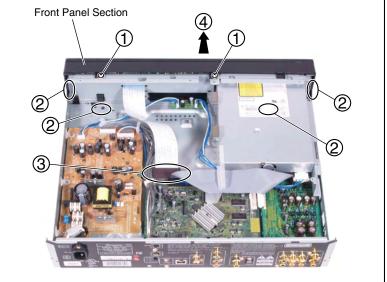
В

С

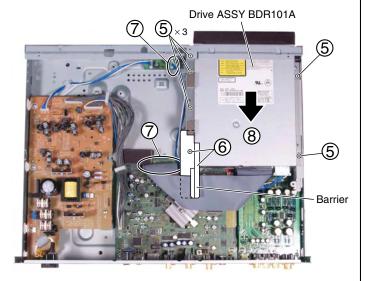
D

Е

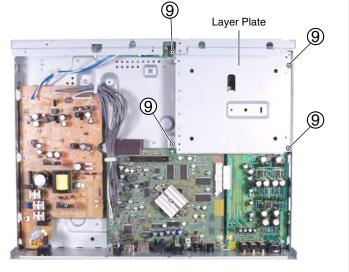
- 3 Disconnect the connector.
- 4 Remove the Front Panel Section.



- (5) Remove the five screws.
- (6) Remove the screw and then remove the styling sheet.
- (7) Disconnect the two connectors.
- (8) Remove the Drive ASSY BDR101A.



- Remove the four screws.
- (10) Remove the Layer Plate.



1

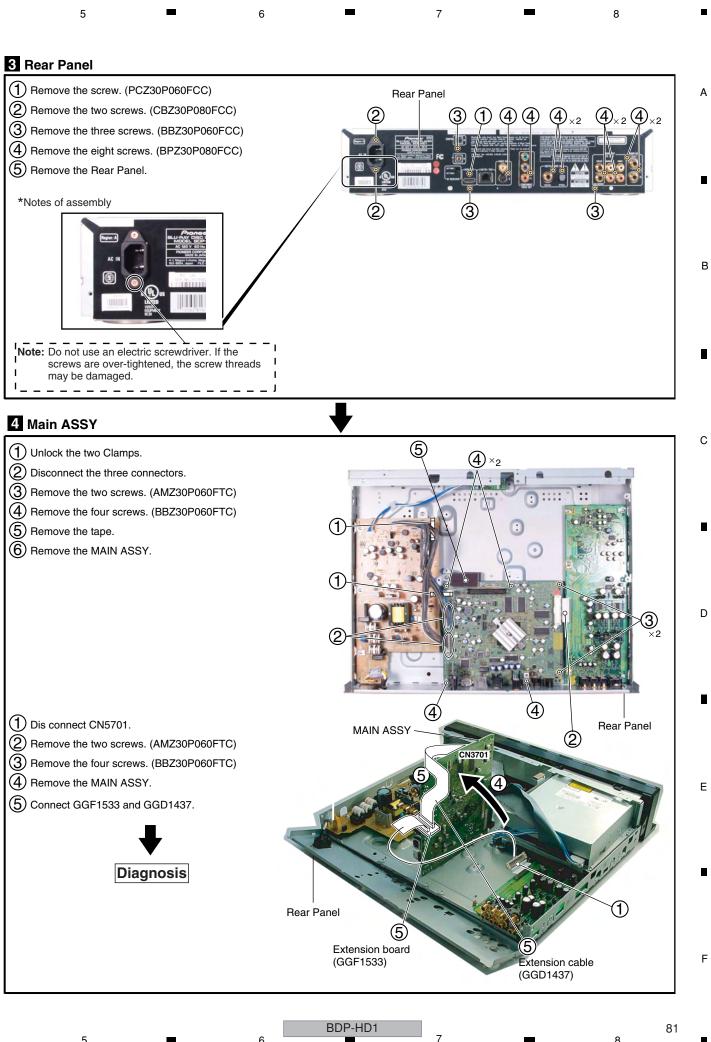
_

80

2

BDP-HD1

_



7.3 PARTS

7.3.1 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

List of IC

SMP8634LF-A, SM5302AS, RTL8201CP-LF, K4H510838C, K4H511638C, PCM1738EG

■ SMP8634LF-A (IC1001)

MAIN LSI

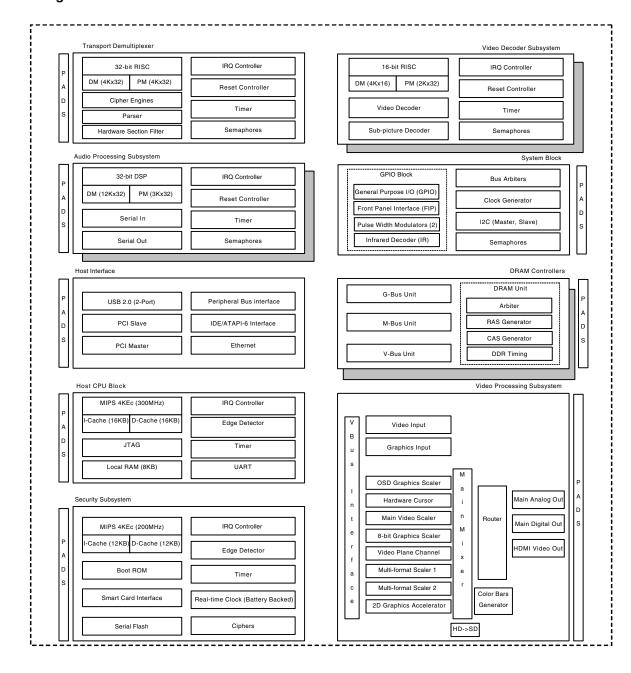
В

С

D

Ε

Block Diagram



BDP-HD1

82

2

3

В

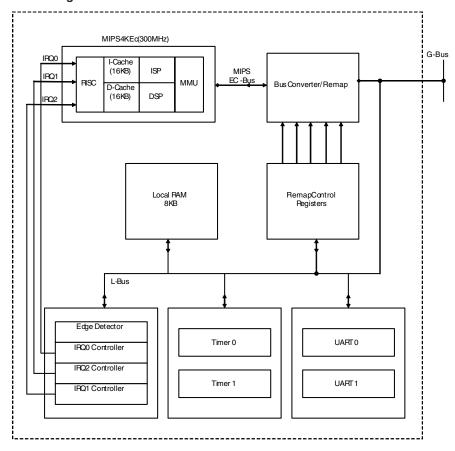
С

D

Е

8

Block Diagram



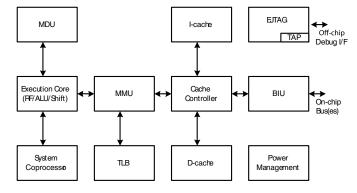
6

■ HOST CPU BLOCK

5

4KEc Core

Block Diagram



BDP-HD1

6

7

8

1 2 3 4

■ HOST CPULBOCK

- Interrupt Controller
- Block Diagram

Α

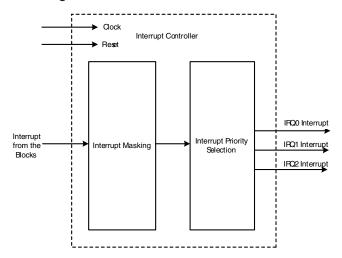
В

С

D

Е

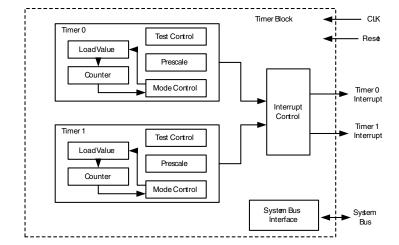
F



■ HOST CPU BLOCK

Timer

Block Diagram

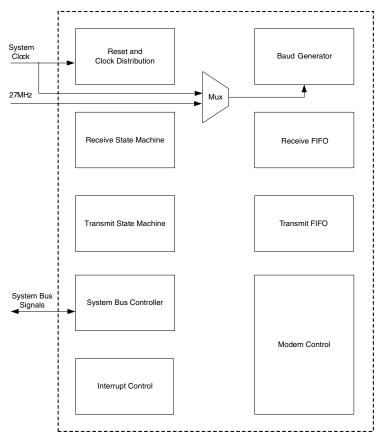


84

BDP-HD1

2

Block Diagram



6

7

8

Α

В

С

D

Ε

F

Pin Function

5

Pin Name	Ball ID	Direction	Description
UARTO_CTS	B14	В	UART 0 clear to send. Flow control signal.
UART0_DCD	B12	В	UART 0 data carrier detect, Data set status signal,
UARTO_DSR	C14	В	UART 0 data set ready. Data set status signal.
UARTO_DTR	C13	В	UART 0 data terminal ready. Data terminal status signal.
UARTO_RTS	B13	В	UART 0 request to send. Flow control signal.
UARTO_RX	A14	В	UART 0 receive data input
UARTO_TX	A13	В	UART 0 transmit data output
UART1_CTS	C12	В	UART 1 clear to send. Flow control signal.
UART1_DCD	C11	В	UART 1 data carrier detect. Data set status signal.
UART1_DSR	B11	В	UART 1 data set ready. Data set status signal.
UART1_DTR	C10	В	UART 1 data terminal ready. Data terminal status signal.
UART1_RTS	B10	В	UART 1 request to send. Flow control signal.
UART1_RX	A12	В	UART 1 receive data input
UART1_TX	A11	В	UART 1 transmit data output

6

BDP-HD1

8

■ SECURITY SUBSYSTEM

Block Diagram

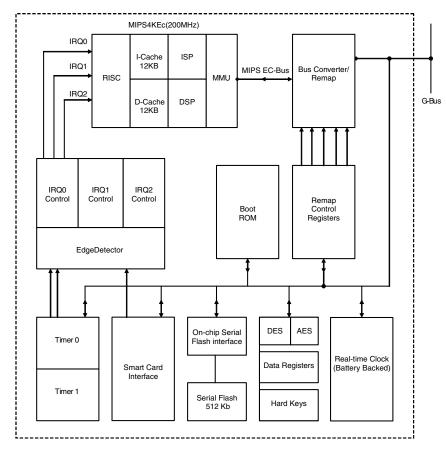
Α

В

С

D

Е



■ SECURITY SUBSYSTEM

• Real-time Clock

Pin Function

Pin Name	Ball ID	Direction	Description
RTC_CLK_IN	AN24	I	Reserved. Make no connection to this pin (internal pull-down).
RTC_CLK_OUT	AP23	0	RTC clock output
RTC_RING	AM24	0	RTC ring output
RTC_TEST	AM25	I	RTC test input
RTC_VDD_BAT_3V3	AL24	I	RTC crystal oscillator power (3.3V)
RTC_VDD_BAT_3V3	AL25	I	RTC battery power (3.3V)
RTC_VSS	AK24	I	RTC crystal oscillator ground
RTC_XTAL_DISC	AN25	I	Reserved. Make no connection to this pin (internal pull-down).
RTC_XTAL_IN	AP24	I	RTC 32KHz crystal oscillator input
RTC_XTAL_OUT	AP25	0	RTC 32KHz crystal oscillator output

F

86

2

BDP-HD1

3

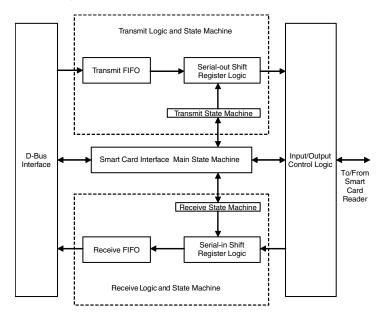
■ 6 **■** 7 **■** 8

■ SECURITY SUBSYSTEM

Smart Card Interface

5

Block Diagram



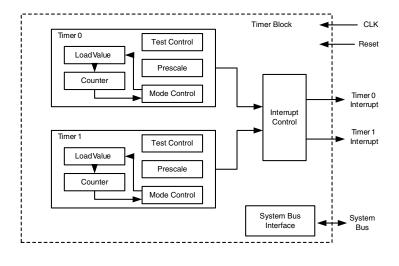
Pin Function

Pin Name	Ball ID	Direction	Description
SCARD_CLK	A16	0	Smart card clock
SCARD_CTL0	C15	В	Smart card control 1
SCARD_CTL1	D16	В	Smart card control 2
SCARD_CTL2	E16	В	Smart card control 3
SCARD_FC#	B16	0	Smart card function code
SCARD_IO	A15	В	Smart card IO
SCARD_RST	B15	0	Smart card reset

■ SECURITY SUBSYSTEM

Timer

Block Diagram



BDP-HD1

7

87

8

Α

В

С

D

Ε

5

2 - 3 - 4

■ SECURITY SUBSYSTEM

• Interrupt Controller

Block Diagram

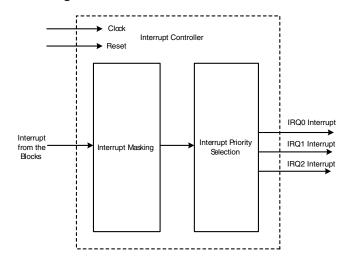
Α

В

С

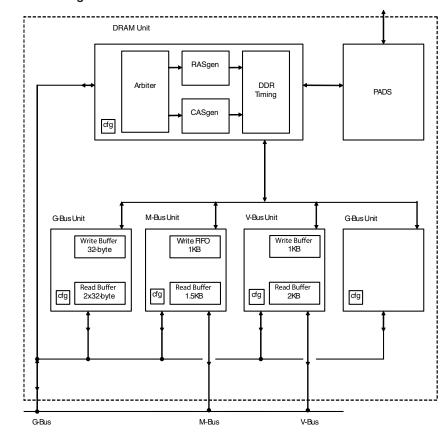
D

Е



■ DRAM CONTROLLER

Block Diagram



88

F

BDP-HD1 3 ■

Pin Name	Ball Id	Direction	Description
DRAM0_A0	V34	0	Memory address bit 0
DRAM0_A1	V33	0	Memory address bit 1
DRAMO_A10	U32	0	Memory address bit 10
DRAMO_A11	T30	0	Memory address bit 11
DRAM0_A12	R31	0	Memory address bit 12
DRAMO_A13	R33	0	Memory address bit 13. Memory address bus provides the SDRAM with the row address for the active commands, and the column address and the auto-precharge value for read/write commands.
DRAM0_A2	V32	0	Memory address bit 2
DRAM0_A3	W31	0	Memory address bit 3
DRAM0_A4	W30	0	Memory address bit 4
DRAM0_A5	V31	0	Memory address bit 5
DRAM0_A6	V30	0	Memory address bit 6
DRAM0_A7	U31	0	Memory address bit 7
DRAM0_A8	U30	0	Memory address bit 8
DRAM0_A9	T31	0	Memory address bit 9
DRAMO_BA0	U34	0	Bank address output 0
DRAM0_BA1	U33	0	Bank address output 1. BA[1:0] define to which SDRAM bank an active, read, write or precharge command is being applied.
DRAMO_CAS#	T34	0	Column address strobe. Memory command output. In conjunction with CAS# and WE#, this signal determines the memory operation requested (active-low).
DRAM0_CK	K34	0	Non-inverted clock output. CK and CK# are a differential clock signal pair. The SDRAM0 address and control signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. SDRAM output (read) data is referenced to the crossings of CK and CK# in both directions.
DRAM0_CK#	L34	0	Inverted clock output. CK and CK# are a differential clock signal pair. The SDRAM address and control signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. SDRAM output (read) data is referenced to the crossings of CK and CK# in both directions (active-low).
DRAMO_CKE	R30	0	Clock enable. A high level activates, and a low level deactivates the internal clock signals in the SDRAM. This signal is driven low to activate the SDRAM power-down modes.
DRAM0_DM0	H33	0	Write data mask for bits [07:00] of memory data
DRAM0_DM1	H32	0	Write data mask for bits [15:08] of memory data
DRAM0_DM2	N33	0	Write data mask for bits [23:16] of memory data
DRAMO_DM3	N34	0	Write data mask for bits [31:24] of memory data. Write data is masked when the corresponding DM bit is sampled high by the SDRAM during a write access.
DRAM0_DQ0	K31	В	Memory data bus bit 0 (LSB)
DRAM0_DQ1	K30	В	Memory data bus bit 1
DRAM0_DQ10	G33	В	Memory data bus bit 10
DRAM0_DQ11	G32	В	Memory data bus bit 11
DRAM0_DQ12	G30	В	Memory data bus bit 12
DRAM0_DQ13	G31	В	Memory data bus bit 13
DRAM0_DQ14	F34	В	Memory data bus bit 14

7

Α

8

В

С

D

Е

F

3

Pin Name	Ball Id	Direction	Description
DRAM0_DQ15	F33	В	Memory data bus bit 15
DRAM0_DQ16	R34	В	Memory data bus bit 16
DRAM0_DQ17	P31	В	Memory data bus bit 17
DRAM0_DQ18	P30	В	Memory data bus bit 18
DRAM0_DQ19	P32	В	Memory data bus bit 19
DRAM0_DQ2	K33	В	Memory data bus bit 2
DRAM0_DQ20	P33	В	Memory data bus bit 20
DRAM0_DQ21	P34	В	Memory data bus bit 21
DRAM0_DQ22	N31	В	Memory data bus bit 22
DRAM0_DQ23	N30	В	Memory data bus bit 23
DRAM0_DQ24	M30	В	Memory data bus bit 24
DRAM0_DQ25	M32	В	Memory data bus bit 25
DRAM0_DQ26	M33	В	Memory data bus bit 26
DRAM0_DQ27	M34	В	Memory data bus bit 27
DRAM0_DQ28	L31	В	Memory data bus bit 28
DRAM0_DQ29	L30	В	Memory data bus bit 29
DRAM0_DQ3	K32	В	Memory data bus bit 3
DRAM0_DQ30	L32	В	Memory data bus bit 30
DRAM0_DQ31	L33	В	Memory data bus bit 31 (MSB)
DRAM0_DQ4	J34	В	Memory data bus bit 4
DRAM0_DQ5	J33	В	Memory data bus bit 5
DRAM0_DQ6	J32	В	Memory data bus bit 6
DRAM0_DQ7	J31	В	Memory data bus bit 7
DRAM0_DQ8	H31	В	Memory data bus bit 8
DRAM0_DQ9	G34	В	Memory data bus bit 9
DRAM0_DQS0	H34	В	Data strobes for bits 07:00 of memory data
DRAM0_DQS1	H30	В	Data strobes for bits [15:08] of memory data
DRAM0_DQS2	N32	В	Data strobes for bits [23:16] of memory data
DRAM0_DQS3	M31	В	Data strobes for bits [31:24] of memory data bus. Output by the SMP8634 with the write data; output by the SDRAM with the read data.
DRAM0_RAS#	T33	0	Memory command output. In conjunction with WE#, this signal determines the memory operation requested.
DRAM0_CS#	T32	0	Chip select (active low)
DRAM0_VREFSSTL0	L29	I	SSTL-2 voltage reference input (1.25V)
DRAM0_VREFSSTL1	J30	I	SSTL-2 voltage reference input (1.25V)
DRAM0_VREFSSTL2	G29	I	SSTL-2 voltage reference input (1.25V)
DRAM0_WE#	R32	0	Write enable (active-low). Memory command output. In conjunction with CAS# and WE#, this signal determines the memory operation requested.
DRAM1_A0	B34	0	Memory address bit 0
DRAM1_A1	C34	0	Memory address bit 1
DRAM1_A10	C33	0	Memory address bit 10
DRAM1_A11	E31	0	Memory address bit 11

В

С

D

Ε

F

90

1

BDP-HD1 2

Pin Name	Ball Id	Direction	Description
DRAM1_A13	B31	0	Memory address bit 13. Memory address bus provides the SDRAM with the row address for the active commands, and the column address and the auto-precharge value for read/write commands.
DRAM1_A2	D34	0	Memory address bit 2
DRAM1_A3	E34	0	Memory address bit 3
DRAM1_A4	D33	0	Memory address bit 4
DRAM1_A5	E33	0	Memory address bit 5
DRAM1_A6	D32	0	Memory address bit 6
DRAM1_A7	E32	0	Memory address bit 7
DRAM1_A8	F32	0	Memory address bit 8
DRAM1_A9	D31	0	Memory address bit 9
DRAM1_BA0	A33	0	Bank address output 0
DRAM1_BA1	В33	0	Bank address output 1. BA[1:0] define to which SDRAM bank an active, read, write or precharge command is being applied.
DRAM1_CAS#	A32	0	Column address strobe (active-low). Memory command output. In conjunction with WE#, this signal determines the memory operation requested.
DRAM1_CK	A26	0	Non-inverted clock output. CK and CK# are a differential clock signal pair. SDRAM address an control signals are sampled on the crossing of the positive edge of CK and the negative edge cCK#. SDRAM output (read) data is referenced the crossings of CK and CK# in both directions.
DRAM1_CK#	A27	0	Inverted clock output. CK and CK# are a differential clock signal pair, SDRAM address and cortrol signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. SDRAM output (read) data is referenced the crossings of CK and CK# in both directions (active-low).
DRAM1_CKE	F30	0	Clock enable. A high level activates, and a low level deactivates the internal clock signals in th SDRAM. This signal is driven low to activate the SDRAM power-down modes.
DRAM1_DM0	B24	0	Write data mask for bits [07:00] of memory dat
DRAM1_DM1	C24	0	Write data mask for bits [15:08] of memory dat
DRAM1_DM2	B29	0	Write data mask for bits [23:16] of memory dat
DRAM1_DM3	A29	0	Write data mask for bits [31:24] of memory data. Write data is masked when the corresponding DM bit is sampled high by the SDRAM during a write access.
DRAM1_DQ0	D26	В	Memory data bus bit 0 (LSB)
DRAM1_DQ1	E26	В	Memory data bus bit 1
DRAM1_DQ10	B23	В	Memory data bus bit 10
DRAM1_DQ11	C23	В	Memory data bus bit 11
DRAM1_DQ12	D23	В	Memory data bus bit 12
DRAM1_DQ13	A22	В	Memory data bus bit 13
DRAM1_DQ14	B22	В	Memory data bus bit 14
DRAM1_DQ15	C22	В	Memory data bus bit 15
DRAM1_DQ16	A31	В	Memory data bus bit 16
DRAM1_DQ17	D30	В	Memory data bus bit 17
DRAM1_DQ18	E30	В	Memory data bus bit 18
DRAM1_DQ19	C30	В	Memory data bus bit 19
DRAM1_DQ2	B26	В	Memory data bus bit 2

5

BUD-HU1

91

5

8

8

В

С

D

Ε

Pin Name	Ball Id	Direction	Description
DRAM1_DQ20	B30	В	Memory data bus bit 20
DRAM1_DQ21	A30	В	Memory data bus bit 21
DRAM1_DQ22	D29	В	Memory data bus bit 22
DRAM1_DQ23	E29	В	Memory data bus bit 23
DRAM1_DQ24	E28	В	Memory data bus bit 24
DRAM1_DQ25	C28	В	Memory data bus bit 25
DRAM1_DQ26	B28	В	Memory data bus bit 26
DRAM1_DQ27	A28	В	Memory data bus bit 27
DRAM1_DQ28	D27	В	Memory data bus bit 28
DRAM1_DQ29	E27	В	Memory data bus bit 29
DRAM1_DQ3	C26	В	Memory data bus bit 3
DRAM1_DQ30	C27	В	Memory data bus bit 30
DRAM1_DQ31	B27	В	Memory data bus bit 31 (MSB)
DRAM1_DQ4	A25	В	Memory data bus bit 4
DRAM1_DQ5	B25	В	Memory data bus bit 5
DRAM1_DQ6	C25	В	Memory data bus bit 6
DRAM1_DQ7	D25	В	Memory data bus bit 7
DRAM1_DQ8	D24	В	Memory data bus bit 8
DRAM1_DQ9	A23	В	Memory data bus bit 9
DRAM1_DQS0	A24	В	Data strobes for bits 07:00 of memory data
DRAM1_DQS1	E24	В	Data strobes for bits [15:08] of memory data
DRAM1_DQS2	C29	В	Data strobes for bits [23:16] of memory data
DRAM1_DQS3	D28	В	Data strobes for bits [31:24] of memory data bus. Output by the SMP8634 with the write data; output by the SDRAM with the read data.
DRAM1_RAS#	B32	0	DRAM1 row address strobe (active-low). Memory command output. In conjunction with CAS# and WE#, this signal determines the memory operation requested.
DRAM1_CS#	C32	0	DRAM1 chip select (active-low).
DRAM1_VREFSSTL0	F28	I	SSTL-2 voltage reference input (1.25V)
DRAM1_VREFSSTL1	E25	I	SSTL-2 voltage reference input (1.25V)
DRAM1_VREFSSTL2	E23	Ī	SSTL-2 voltage reference input (1,25V)
DRAM1_WE#	C31	0	DRAM1 write enable (active-low). Memory command output. In conjunction with CAS# and WE#, this signal determines the memory operation requested.

92

Ε

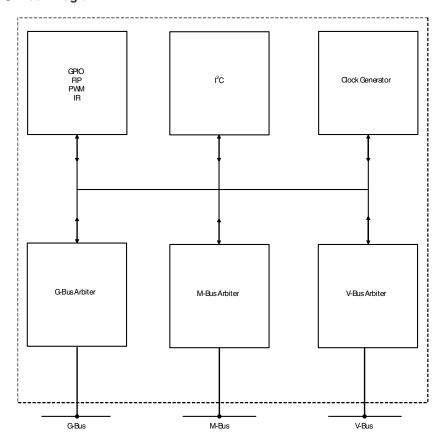
В

С

D

•

3

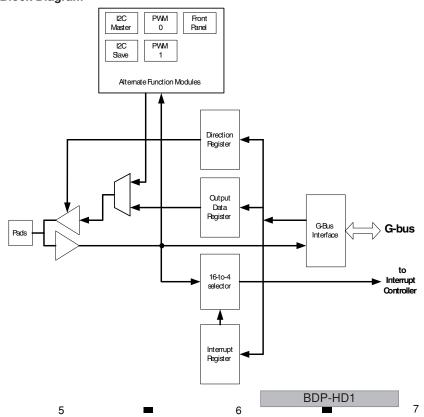


6

7

■ SYSTEM BLOCK • LBC General

Block Diagram



Α

8

В

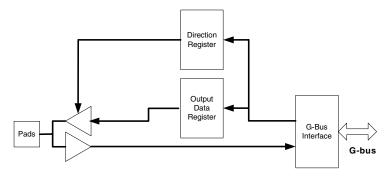
С

D

Ε

■ SYSTEM BLOCK • HBCGeneral

Block Diagram



■ SYSTEM BLOCK

• General Purpose I/O (GPIO)

Pin Function

В

С

D

Е

F

Pin Name	Ball ID	Direction	Description
GPIO0	A5	В	General-purpose IO pin 0
			Alternate function: Master I ² C.
GPIO1	B5	В	General-purpose IO pin 1
			Alternate function: Master I ² C.
GPIO10	E6	В	General-purpose IO pin 10 Selectable input: (PCI) Interrupt Input C,
GPIO11	E8	В	General-purpose IO pin 11 Selectable input: (PCI) Interrupt Input D.
GPIO12	В7	В	General-purpose IO pin 12 Selectable input: Infrared Remote input.
GPIO13	C7	В	General-purpose IO pin 13
GPIO14	D7	В	General-purpose IO pin 14
			Alternate function: PWM generator 1.
GPIO15	E7	В	General-purpose IO pin 15
			Alternate function: PWM generator 0.
GPIO16	AF5	В	General-purpose IO pin 16
GPIO17	AF4	В	General-purpose IO pin 17
GPIO18	AF3	В	General-purpose IO pin 18
GPIO19	AF2	В	General-purpose IO pin 19
GPIO2	C5	В	General-purpose IO pin 2
			Alternate function: Front Panel Interface (FIP).
GPIO20	AE5	В	General-purpose IO pin 20
GPIO21	AE4	В	General-purpose IO pin 21
GPIO22	AE3	В	General-purpose IO pin 22
GPIO23	AE2	В	General-purpose IO pin 23
GPIO24	AD5	В	General-purpose IO pin 24
GPIO25	AD4	В	General-purpose IO pin 25
GPIO26	AD3	В	General-purpose IO pin 26
GPIO27	AD2	В	General-purpose IO pin 27
GPIO28	AC5	В	General-purpose IO pin 28
GPIO29	AC4	В	General-purpose IO pin 29

QΛ

2

BDP-HD1

4

Pin Name	Ball Id	Direction	Description
GPIO3	D5	В	General-purpose IO pin 3
			Alternate function: Front Panel Interface (FIP).
GPIO30	AB5	В	General-purpose IO pin 30
GPIO31	AB4	В	General-purpose IO pin 31
GPIO4	D4	В	General-purpose IO pin 4
			Alternate function: Front Panel Interface (FIP).
GPIO5	E4	В	General-purpose IO pin 5
			Alternate function: Front Panel Interface (FIP).
GPIO6	E5	В	General-purpose IO pin 6
			Alternate function: Slave I ² C.
GPIO7	В6	В	General-purpose IO pin 7
			Alternate function: Slave I ² C.
GPIO8	C6	В	General-purpose IO pin 8
			Selectable input: (PCI) Interrupt Input A.
GPIO9	D6	В	General-purpose IO pin 9
			Selectable input: (PCI) Interrupt Input B.

7

8

Α

В

С

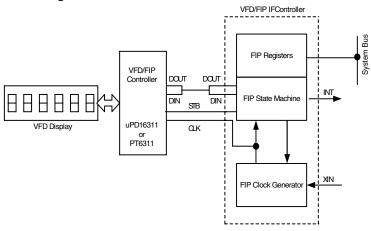
D

Е

■ SYSTEM BLOCK
• Front Panel Controller Interface (FIP)

Block Diagram

5



Pin Function

Pin Name	Ball ID	Direction	Description
GPIO2	C5	В	FIP serial data input
GPIO3	D5	В	FIP serial data output
GPIO4	D4	В	FIP data strobe
GPIO5	E4	В	FIP serial I/O clock

BDP-HD1

8

95

■ 2 **■** 3 **■** 4

■ SYSTEM BLOCK • Infrared Decoder

Block Diagram

Α

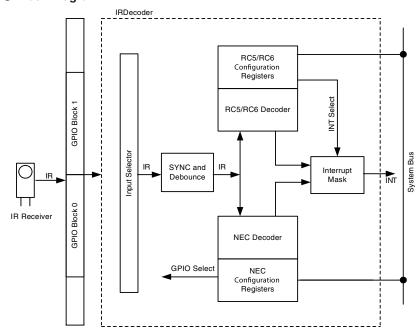
В

С

D

Е

F



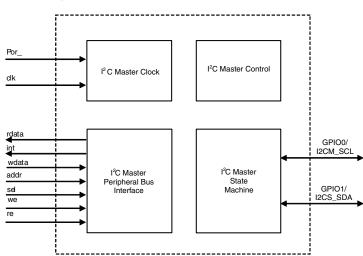
Pin Function

Pin Name	Ball ID	Direction	Description
GPIO12	В7	В	Default pin assigned to the IR decoder input function (may be mapped to any other GPIO pin under the software control).

■ SYSTEM BLOCK

• |2 C Master

Block Diagram



96

2

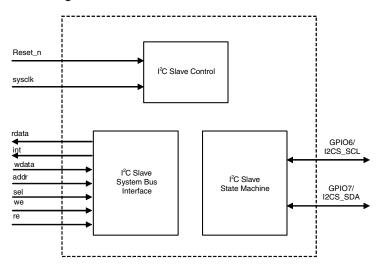
BDP-HD1

■ 6 **■** 7 **■** 8

■ SYSTEM BLOCK • I²C Slave

Block Diagram

5



■SYSTEM BLOCK

•I²C Master and Slave Interface

Pin Function

5

Pin Name	Ball ID	Direction	Description
GPIO0	A5	В	I2CM_SCL, I ² C master interface serial clock
GPIO1	B5	В	I2CM_SDA. I ² C master interface serial data
GPIO6	E5	В	I2CS_SCL, I ² C slave interface serial clock
GPIO7	В6	В	I2CS_SDA. I ² C slave interface serial data

6

BDP-HD1 7 **-**

97

8

Α

В

I

С

D

Е

F

2 3 4

■ SYSTEM BLOCK • Clock Generator

Block Diagram

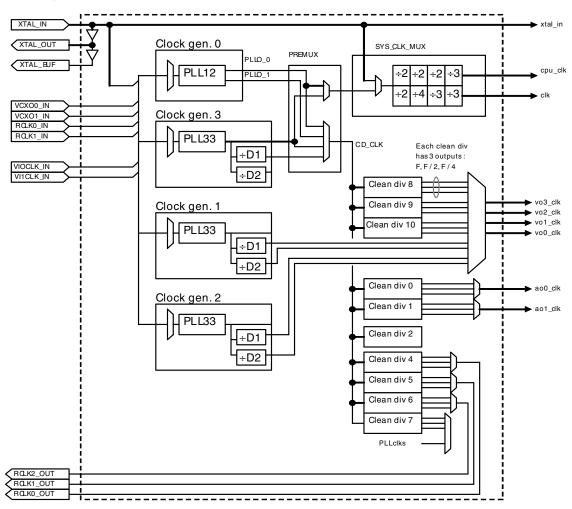
В

С

D

Ε

F



Pin Function

Pin Name	Ball ID	Direction	Description
XTAL_IN	A10	I	27MHz crystal oscillator input
XTAL_OUT	A9	0	Crystal oscillator output
XTAL_BUF	В9	0	Buffered crystal oscillator output
VCXO0_IN	C9	I	Input from external VCXO #0
VCXO1_IN	C8	I	Input from external VCXO #1
RCLK0_IN	В8	I	PLL reference clock input #0
RCLK0_OUT	D8	0	PLL reference clock output #0
RCLK1_OUT	D9	0	Auxiliary clock output #1
RCLK1_XTAL_IN	A7	I	Crystal oscillator input
RCLK1_XTAL_OUT	A6	0	Crystal oscillator output

2

BDP-HD1

98

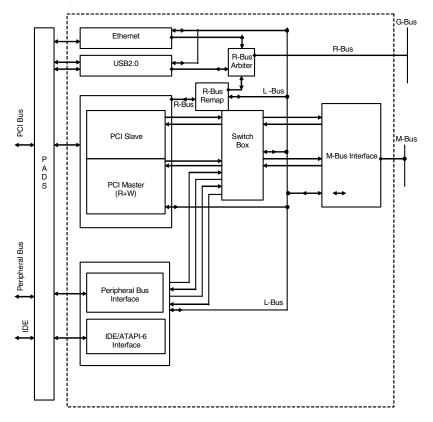
_

3

■ HOST INTERFACE

5

Block Diagram



■ HOST INTERFACE • System Bus

Pin Function

Pin name	Ball ID	Direction	Description
PCI_AD0	AL19	В	PCI address/data pin 0 (LSB)
PCI_AD1	AN19	В	PCI address/data pin 1
PCI_AD10	AN17	В	PCI address/data pin 10
PCI_AD11	AL17	В	PCI address/data pin 11
PCI_AD12	AM17	В	PCI address/data pin 12
PCI_AD13	AL16	В	PCI address/data pin 13
PCI_AD14	AN16	В	PCI address/data pin 14
PCI_AD15	AK16	В	PCI address/data pin 15
PCI_AD16	AK15	В	PCI address/data pin 16
PCI_AD17	AP14	В	PCI address/data pin 17
PCI_AD18	AK14	В	PCI address/data pin 18
PCI_AD19	AP13	В	PCI address/data pin 19
PCI_AD2	AK19	В	PCI address/data pin 2
PCI_AD20	AL13	В	PCI address/data pin 20
PCI_AD21	AN13	В	PCI address/data pin 21
PCI_AD22	AM14	В	PCI address/data pin 22
PCI_AD23	AN12	В	PCI address/data pin 23

6

BDP-HD1

99

Α

В

С

D

Е

F

5

_

Pin name Ball ID Direction Description PCI AD24 AL11 В PCI address/data pin 24 PCI_AD25 AN11 В PCI address/data pin 25 PCI_AD26 AM12 В PCI address/data pin 26 PCI_AD27 AP11 В PCI address/data pin 27 PCI_AD28 AL10 В PCI address/data pin 28 PCI_AD29 AN10 В PCI address/data pin 29 PCI_AD3 AM19 В PCI address/data pin 3 PCI_AD30 AM11 В PCI address/data pin 30 PCI address/data pin 31 (MSB). The address and the data are multiplexed on the AD pins during the memory and the I/O operations on the PCI PCI_AD31 AP10 В PCI_AD4 AK17 В PCI address/data pin 4 PCI_AD5 AP18 В PCI address/data pin 5 PCI_AD6 В AK18 PCI address/data pin 6 PCI_AD7 AN18 В PCI address/data pin 7 PCI_AD8 AP17 В PCI address/data pin 8 PCI AD9 AM18 В PCI address/data pin 9 PCI CBE0# В AL18 Command/byte enable pin 0. Applies to PCI_AD(7:0). Command/byte enable pin 1. Applies to PCI_AD(15:8). PCI CBE1# AP16 В PCI_CBE2# В AN14 Command/byte enable pin 2. Applies to PCI_AD(23:16). PCI_CBE3# В Command/byte enable pin 3. During the address phase of a transaction the CBE(3:0)# defines the AP12 PCI command. During the data phase each signal indicates whether the associated data byte will be transferred. The CBE3# applies to PCI_AD(31:24). PCI_CLK AP8 Ι Clock input for PCI interface section. Either 33MHz or a 66MHz clock signal. В PCI_DEVSEL# AP15 Device select pin. A target asserts DEVSEL# when it decodes its address. PCI_FRAME# Cycle frame pin. Current initiator asserts the FRAME# pin to indicate the start and duration of a AL14 В transaction PCI_GNTB0 AP9 0 PCI host mode: Bus grant for master #0. Asserted low to grant the PCI ownership to an external master. PCI device mode: Bus request output to an external PCI host. PCI host mode: Bus grant for master #1. Asserted low to grant the PCI ownership to an external master. PCI_GNTB1 AN9 0 PCI device mode: Unused, make no connection. PCI GNTB2 AM10 0 PCI host mode: Bus grant for master #2. Asserted low to grant the PCI ownership to an external master.

F

В

С

D

Ε

BDP-HD1

external master.

PCI device mode: Unused, make no connection.

PCI host mode: Bus grant for master #3.

Asserted low to grant the PCI ownership to an

PCI device mode: Unused, make no connection.

PCI host mode: ID select for PCI device #0. Asserted low by the SMP8634 to indicate a configuration cycle to a PCI device.
PCI device mode: Asserted low by an external PCI

host to indicate a configuration cycle for the SMP8634.

100

PCI_GNTB3

PCI_IDSEL0

AM9

AM13

2

5 **-** 6 **-** 7

Pin name	Ball ID	Direction	Description
PCI_IDSEL1	AL12	0	PCI host mode: ID select for PCI device #1. Asserted low by the SMP8634 to indicate a configuration cycle to a PCI device. PCI Device Mode: Unused, make no connection.
			Tel Device Flode: Olidsed, Make No connection,
PCI_IDSEL2	AK12	0	PCI host mode: ID Select for the PCI device #2. Asserted low by the SMP8634 to indicate a config- uration cycle to a PCI device.
			PCI device mode: Unused, make no connection.
PCI_IDSEL3	AK13	0	PCI host mode: ID Select for the PCI device #3. Asserted low by the SMP8634 to indicate a configuration cycle to a PCI device.
			PCI device mode: Unused, make no connection.
PCI_INTA#	AN8	В	Interrupt A pin. Asserted by a PCI agent to request an interrupt.
PCI_IRDY#	AM15	В	Initiator ready pin. The current bus master asserts IRDY# to indicate that it is ready to complete a transaction.
PCI_PAR	AM16	В	Parity, Driven by an initiator (write) or currently-addressed target (read) to create even parity across AD(31:0) and CBE(3:0)#.
PCI_REQ0#	AL9	I	PCI host mode: Bus request for master #0. Asserted low by an external master requesting a PCI bus transaction.
			PCI device mode: Bus grant input from an external PCI host.
PCI_REQ1#	AK9	I	PCI Host Mode: Bus Request for Master #1. Asserted low by external master requesting PCI bus transaction.
			PCI Device Mode: Unused, make no connection.
PCI_REQ2#	AK10	I	PCI host mode: Bus Request for master #2. Asserted low by external master requesting PCI bus transaction.
			PCI Device Mode: Unused, make no connection.
PCI_REQ3#	AK11	I	PCI host mode: Bus Request for master #3. Asserted low by external master requesting PCI bus transaction.
			PCI Device Mode: Unused, make no connection.
PCI_STOP#	AN15	0	Stop pin. Asserted by an addressed target to request the bus master to terminate the current transaction in progress.
PCI_TRDY#	AL15	В	Target ready pin. The currently addressed target asserts TRDY# to indicate that it is ready to complete a transaction.

■ HOST INTERFACE • USB 2.0

Pin Function

Pin Name	Ball ID	Direction	Description
USB20_ATEST	AN23	В	USB 2.0 analog test I/O
USB20_DM_0	AP21	В	USB 2.0 line interface - port 0 -DM
USB20_DM_1	AP22	В	USB 2.0 line interface - port 1 -DM
USB20_DP_0	AN21	В	USB 2.0 line interface - port 0 -DP
USB20_DP_1	AN22	В	USB 2.0 line interface - port 1 -DP
USB20_REXT	AN20	В	USB 2.0 bias resistor input
USB20_VSST_0	AL20	I	USB 2.0 ground
USB20_VSSC	AL21	I	USB 2.0 ground
USB20_VDD33C	AL22	I	USB 2.0 analog power supply (3.3V)
USB20_VSST_1	AL23	I	USB 2.0 ground
USB20_VDD33T_0	AM20	I	USB 2.0 analog power supply (3.3V)

BDP-HD1

7

101

8

Α

В

С

D

Ε

F

	2	3	4

Pin name	Ball ID	Direction	Description
USB20_VDD33T_0	AM21	I	USB 2.0 analog power supply (3.3V)
USB20_VDD33T_0	AM22	I	USB 2.0 analog power supply (3.3V)
USB20_VDD33T_1	AM23	I	USB 2.0 analog power supply (3.3V)
USB20_VSST_0	AK20	I	USB 2.0 ground
USB20_VSST_0	AK21	I	USB 2.0 ground
USB20_VSST_1	AK22	I	USB 2.0 ground
USB20_VSST_1	AK23	I	USB 2.0 ground
USB20_XI	AP20	I	USB 2.0 Xtal oscillator input (optional)
USB20_XO	AP19	0	USB 2.0 Xtal oscillator output (optional)

■ HOST INTERFACE

• MII Interface

Pin Function

В

С

D

Ε

Pin Name	Ball ID	Direction	Description
ETH_COL	AC3	В	Ethernet collision detect/GPIO14
ETH_CRS	AA3	В	Ethernet carrier sense/GPIO13
ETH_MDC	AD1	В	Ethernet management data clock/GPIO15
ETH_MDINT#	AA5	В	Ethernet management interrupt/GPIO17
ETH_MDIO	Y4	В	Ethernet management data I/O/GPIO16
ETH_RX_DV	AE1	В	Ethernet receive data valid /GPIO7
ETH_RX_ER	AF1	В	Ethernet receive error/GPIO8
ETH_RXCLK	AC2	В	Ethernet receive clock/GPIO6
ETH_RXD0	AC1	В	Ethernet receive data 0/GPIO9
ETH_RXD1	AB3	В	Ethernet receive data 1/GPIO10
ETH_RXD2	AB2	В	Ethernet receive data 2/GPIO11
ETH_RXD3	AB1	В	Ethernet receive data 3/GPIO12
ETH_TX_EN	AA2	В	Ethernet transmit enable/GPIO1
ETH_TXCLK	AA1	В	Ethernet transmit clock/GPIO0
ETH_TXD0	Y3	В	Ethernet transmit data 0/GPIO2
ETH_TXD1	Y2	В	Ethernet transmit data 1/GPIO3
ETH_TXD2	Y1	В	Ethernet transmit data 2/GPIO4
ETH_TXD3	W1	В	Ethernet transmit data 3/GPIO5

■ HOST INTERFACE
• Peripheral Bus Interface (PBI)

● Block Diagram

AUTO PBI Peripheral Bus →G-Bus L-Bus 🔫

102

BDP-HD1

■ HOST INTERFACE • PBI Control

Pin Function

5

Signal	Direction	Description
PB_CS#[3:0]	0	Four chip selects (active low)
PB_RD#	0	Read strobe (active low)
PB_WR#	0	Write strobe (active low)
PB_IORDY#	I	Ready - An accessed device can extend the PB transaction by pulling this line low through an open collector.
PB_ALE	0	Address latch enable. In multiplexed address/data mode, this signal indicates when to latch the address.
PB_DIR#	0	Indicates the direction of the current transaction (may be used to control external transceivers).
PB_DMAREQ	I	An external IDE device can request a DMA transfer using this signal
PB_DMAACK	0	DMA acknowledge

■ HOST INTERFACE

•PBI

Pin Function

Pin Name	Ball ID	Direction	Description
PB_A0	AM32	0	PBI address bit 0 (LSB)
PB_A1	AN32	0	PBI address bit 1
PB_A10	AN30	0	PBI address bit 10
PB_A11	AP30	0	PBI address bit 11
PB_A12	AK29	0	PBI address bit 12
PB_A13	AL29	0	PBI address bit 13
PB_A14	AM29	0	PBI address bit 14
PB_A15	AN29	0	PBI address bit 15 (MSB). Provides address for non-multiplexed bus cycles.
PB_A16	AP29	0	PBI address bit 16
PB_A17	AL28	0	PBI address bit 17
PB_A18	AM28	0	PBI address bit 18
PB_A19	AN28	0	PBI address bit 19
PB_A2	AP32	0	PBI address bit 2
PB_A20	AP28	0	PBI address bit 20
PB_A21	AL27	0	PBI address bit 21
PB_A22	AM27	0	PBI address bit 22
PB_A23	AN27	0	PBI address bit 23
PB_A24	AP27	0	PBI address bit 24
PB_A3	AM31	0	PBI address bit 3
PB_A4	AN31	0	PBI address bit 4
PB_A5	AP31	0	PBI address bit 5
PB_A6	AJ30	0	PBI address bit 6
PB_A7	AK30	0	PBI address bit 7
PB_A8	AL30	0	PBI address bit 8

BDP-HD1

5

103

Α

В

С

D

Е

F

■ 2 **■** 3

Pin Name Ball ID Direction Description PB_A9 AM30 0 PBI address bit 9 PB_AD0 AK34 В Multiplexed address/data bit 0 (LSB) PB_AD1 AK33 В Multiplexed address/data bit 1 PB_AD10 AH32 В Multiplexed address/data bit 10 PB_AD11 AH31 В Multiplexed address/data bit 11 PB_AD12 AJ34 В Multiplexed address/data bit 12 PB_AD13 AJ33 В Multiplexed address/data bit 13 PB_AD14 В AJ32 Multiplexed address/data bit 14 PBI multiplexed address/data bit 15 (MSB). Used as multiplexed address and data bus for 16/16mux and 24/8 mux modes. Used as a data bus in 24/8 and 16/16 modes. AD(7:0) forms loworder byte of address in 24/8 mode. PB_AD15 AJ31 В PB_AD2 AK32 В Multiplexed address/data bit 2 PB_AD3 В AK31 Multiplexed address/data bit 3 PB_AD4 AL34 В Multiplexed address/data bit 4 PB_AD5 AL33 В Multiplexed address/data bit 5 PB_AD6 AL32 В Multiplexed address/data bit 6 PB_AD7 AL31 В Multiplexed address/data bit 7 В PB_AD8 AH34 Multiplexed address/data bit 8 В PB_AD9 **AH33** Multiplexed address/data bit 9 0 PB_ALE AG30 Address latch enable PB_CS0# AG34 0 Chip select #0 (active low) PB_CS1# AG33 0 Chip select #1 (active low) PB_CS2# О AG32 Chip select #2 (active low) PB_CS3# AG31 О Chip select #3 (active low). Pins PB_CSB3:0 become active for accesses to specified regions of the PB memory space. PB_DIR# AH30 О Transfer direction (low = read, high = write) PB_DMACK# AM33 0 DMA acknowledge I PB_DMARQ AN33 DMA request Device ready. A device can extend a transfer cycle by pulling this line low prior to the IORDY sampling point, and holding it low until the device is ready to complete the cycle. I PB_IORDY AP33 PB_RD# AM34 0 Read command (active low) PB_WR# AN34 0 Write command (active low)

104

В

С

D

Ε

F

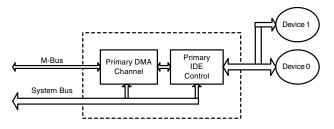
BDP-HD1

2 3 •

■ HOST INTERFACE • IDE/ATAPI-6 Interface

Block Diagram

5



Pin Function

Pin Name	Ball ID	Direction	Description
IDE_CS0#	D22	0	Chip select #0
IDE_CS1#	E22	0	Chip select #1
IDE_DACK#	C20	0	DMA acknowledge
IDE_DMARQ	D20	I	DMA request
IDE_A0	B21	0	IDE bus address bit 0
IDE_A1	E21	0	IDE bus address bit 1
IDE_A2	C21	0	IDE bus address bit 2
IDE_D0	C19	В	IDE data bit 0 (LSB)
IDE_D1	A19	В	IDE data bit 1
IDE_D10	B17	В	IDE data bit 10
IDE_D11	D18	В	IDE data bit 11
IDE_D12	A18	В	IDE data bit 12
IDE_D13	C18	В	IDE data bit 13
IDE_D14	E19	В	IDE data bit 14
IDE_D15	B19	В	IDE data bit 15 (MSB)
IDE_D2	D19	В	IDE data bit 2
IDE_D3	B18	В	IDE data bit 3
IDE_D4	E18	В	IDE data bit 4
IDE_D5	C17	В	IDE data bit 5
IDE_D6	A17	В	IDE data bit 6
IDE_D7	D17	В	IDE data bit 7
IDE_D8	C16	В	IDE data bit 8
IDE_D9	E17	В	IDE data bit 9
IDE_IOR#	A20	0	Read command (active-low)
IDE_IOW#	E20	0	Write command (active-low)
IDE_INTRQ	D21	I	IDE device interrupt request
IDE_IORDY	B20	I	IDE cycle extension input
IDE_NPCBLID	A21	I	Cable ID input. Used to detect the type of cable assembly in use.

BDP-HD1

8

Α

В

С

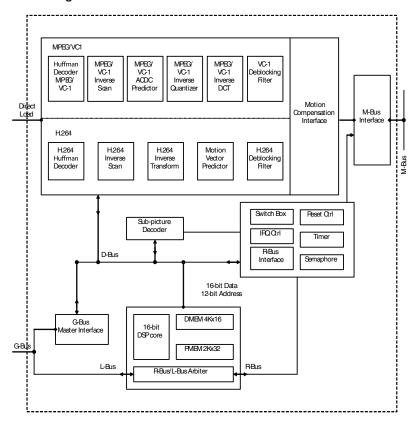
D

Е

F

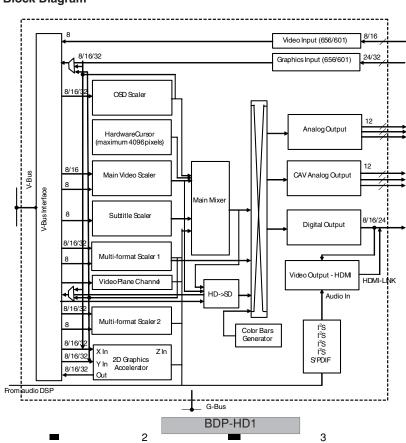
■ VIDEO DECODER SUBSYSTEM

Block Diagram



■ VIDEO PROCESSING SUBSYSTEM

Block Diagram



106

В

С

D

Е

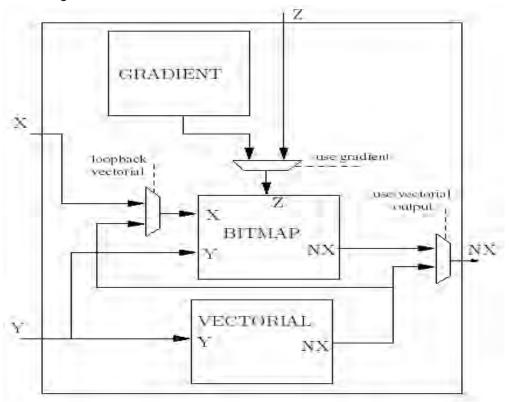
F

■ VIDEO PROCESSING SUBSYSTEM

Graphics Accelerator

Block Diagram

5



■ VIDEO PROCESSING SUBSYSTEM

• Digital Video Input 0 (Graphic Input)

Pin Function

Pin Name	Ball ID	Direction	Description
VI0_CLK	K1	I	Video graphic input port 0 clock
VIO_HS	J2	В	Video graphic input port 0 Hsync
VIO_PO	D2	I	Video graphic input port 0 bit 0
VI0_P1	D1	I	Video graphic input port 0 bit 1
VI0_P10	G5	I	Video graphic input port 0 bit 10
VI0_P11	G4	I	Video graphic input port 0 bit 11
VI0_P12	G3	I	Video graphic input port 0 bit 12
VI0_P13	G2	I	Video graphic input port 0 bit 13
VI0_P14	G1	I	Video graphic input port 0 bit 14
VI0_P15	H5	I	Video graphic input port 0 bit 15
VI0_P16	H4	I	Video graphic input port 0 bit 16
VI0_P17	Н3	I	Video graphic input port 0 bit 17
VI0_P18	H2	I	Video graphic input port 0 bit 18
VI0_P19	H1	I	Video graphic input port 0 bit 19
VIO_P2	E3	I	Video graphic input port 0 bit 2
VI0_P20	J5	I	Video graphic input port 0 bit 20
VI0_P21	J4	I	Video graphic input port 0 bit 21

6

BDP-HD1

7

107

Α

В

С

D

Е

5

Pin Name	Ball ID	Direction	Description
VIO_P22	J3	I	Video graphic input port 0 bit 22
VIO_P23	K5	I	Video graphic input port 0 bit 23
VIO_P24	K4	I	Video graphic input port 0 bit 24
VIO_P25	К3	I	Video graphic input port 0 bit 25
VIO_P26	L5	I	Video graphic input port 0 bit 26
VIO_P27	L4	I	Video graphic input port 0 bit 27
VIO_P28	L3	I	Video graphic input port 0 bit 28
VI0_P29	M5	I	Video graphic input port 0 bit 29
VIO_P3	E2	I	Video graphic input port 0 bit 3
VIO_P30	M4	I	Video graphic input port 0 bit 30
VI0_P31	М3	I	Video graphic input port 0 bit 31
VIO_P4	E1	I	Video graphic input port 0 bit 4
VIO_P5	F5	I	Video graphic input port 0 bit 5
VIO_P6	F4	I	Video graphic input port 0 bit 6
VIO_P7	F3	I	Video graphic input port 0 bit 7
VIO_P8	F2	I	Video graphic input port 0 bit 8
VIO_P9	F1	I	Video graphic input port 0 bit 9
VI0_VLD	K2	I	Video graphic input port 0 data valid
VI0_VS	J1	В	Video graphic input port 0 Vsync

■ VIDEO PROCESSING SUBSYSTEM • Digital Video Input 1

Pin Function

В

С

D

Ε

F

Pin Name	Ball ID	Direction	Description
VI1_CLK	А3	I	Video input port 1 clock signal. Active edge programmable.
VI1_HS	В3	В	Video input port 1 Hsync input or output
VI1_P0	A2	I	Video input port 1 pixel bus bit 0
VI1_P1	B2	I	Video input port 1 pixel bus bit 1
VI1_P2	C3	I	Video input port 1 pixel bus bit 2
VI1_P3	C4	I	Video input port 1 pixel bus bit 3
VI1_P4	B1	I	Video input port 1 pixel bus bit 4
VI1_P5	C1	I	Video input port 1 pixel bus bit 5
VI1_P6	C2	I	Video input port 1 pixel bus bit 6
VI1_P7	D3	I	Video input port 1 pixel bus bit 7
VI1_VLD	B4	I	Video input port 1 data valid
VI1_VS	A4	В	Video input port 1 Vsync input or output

108

■ VIDEO PROCESSING SUBSYSTEM • Digital Video Input 2

Pin Function

5

Pin Name	Ball ID	Direction	Description
VI2_CLK	M1	I	Video input port 2 clock signal. Active edge programmable.
VI2_HS	L2	В	Video input port 2 Hsync input or output
VI2_VLD	M2	I	Video input port 2 data valid
VI2_VS	L1	В	Video input port 2 Vsync input or output

■ VIDEO PROCESSING SUBSYSTEM • Digital Video Output

Pin Function

Pin Name	Ball ID	Direction	Description	
VO0_CLK	U1	0	Video output pixel clock signal	
VO0_HS	V1	В	Video output Hsync input or output. Polarity pro grammable.	
VO0_P0	W3	0	Video output pixel bus bit 0 (YPbPr/RGB)	
VO0_P1	V4	0	Video output pixel bus bit 1 (YPbPr/RGB)	
VO0_P10	R4	0	Video output pixel bus bit 10 (YPbPr/RGB)	
VO0_P11	R3	0	Video output pixel bus bit 11 (YPbPr/RGB)	
VO0_P12	R2	0	Video output pixel bus bit 12 (YPbPr/RGB)	
VO0_P13	R1	0	Video output pixel bus bit 13 (YPbPr/RGB)	
VO0_P14	P5	0	Video output pixel bus bit 14 (YPbPr/RGB)	
VO0_P15	P4	0	Video output pixel bus bit 15 (YPbPr/RGB)	
VO0_P16	Р3	0	Video output pixel bus bit 16 (YPbPr/RGB)	
VO0_P17	P2	0	Video output pixel bus bit 17 (YPbPr/RGB)	
VO0_P18	P1	0	Video output pixel bus bit 18 (YPbPr/RGB)	
VO0_P19	N5	0	Video output pixel bus bit 19 (YPbPr/RGB)	
VO0_P2	V3	0	Video output pixel bus bit 2 (YPbPr/RGB)	
VO0_P20	N4	0	Video output pixel bus bit 20 (YPbPr/RGB)	
VO0_P21	N3	0	Video output pixel bus bit 21 (YPbPr/RGB)	
VO0_P22	N2	0	Video output pixel bus bit 22 (YPbPr/RGB)	
VO0_P23	N1	0	Video output pixel bus bit 23 (YPbPr/RGB)	
VO0_P3	U4	0	Video output pixel bus bit 3 (YPbPr/RGB)	
VO0_P4	U3	0	Video output pixel bus bit 4 (YPbPr/RGB)	
VO0_P5	T4	0	Video output pixel bus bit 5 (YPbPr/RGB)	
VO0_P6	Т3	0	Video output pixel bus bit 6 (YPbPr/RGB)	
VO0_P7	T2	0	Video output pixel bus bit 7 (YPbPr/RGB)	
VO0_P8	T1	0	Video output pixel bus bit 8 (YPbPr/RGB)	
VO0_P9	R5	0	Video output pixel bus bit 9 (YPbPr/RGB)	
VO0_VLD	U2	0	Video output port data valid signal. Active high.	
V00_VS	V2	В	Video output port Vsync input or output. Polarity programmable.	

BDP-HD1

109

5

Α

В

С

D

Ε

Pin Function

Pin Name	Ball ID	Direction	Description
VO1_AVDD	AG4	I	Video output analog block 3.3V power supply connection
VO1_AVDD_U	AJ2	I	Pb-channel DAC power supply. Connect to a 3.3V nominal supply.
VO1_AVDD_V	AH2	I	Pr-channel DAC power supply. Connect to a 3.3V nominal supply.
VO1_AVDD_Y	AG2	I	Y-channel DAC power supply. Connect to a 3.3V nominal supply.
VO1_AVSS	AG5	I	Video output analog block ground connection
VO1_AVSS_U	AJ3	I	Pb-channel DAC ground connection
VO1_AVSS_V	AH3	I	Pr-channel DAC ground connection
VO1_AVSS_Y	AG3	I	Y-channel DAC ground connection
VO1_RSET	AH4	0	DAC current set pin. A resistor (140 ohm, 1% tolerance) connected between this pin and the ground sets the full-scale DAC current.
VO1_U	AJ1	0	Analog video output. Outputs Pb signal in the component YPbPr mode, the composite signal in S-video mode, or B signal in component RGB mode. Current output, intended to drive 75 ohm doubly-terminated load.
VO1_V	AH1	0	Analog video output. Outputs Pr signal in compo- nent YPbPr mode, C (chrominance) signal in S- video mode, or R signal in component RGB mode. Current output, intended to drive 75 ohm doubly- terminated load.
VO1_VREF	AH5	В	Video DAC current source reference voltage (1.25V nominal)
VO1_Y	AG1	0	Analog video output. Output Y (luminance) signals in the component YPbPr or S-video mode, or G signal in the component RGB mode. Current output, intended to drive 75 ohm doubly-terminated load.

■ VIDEO PROCESSING SUBSYSTEM

• Component Analog Output

Pin Function

D

Е

Pin Name	Ball ID	Direction	Description
VO2_AVDD	AK4	I	Video output analog block 3.3V power supply con nection.
VO2_AVDD_U	AM2	I	Pb-channel DAC power supply. Connect to a 3.3V nominal supply.
VO2_AVDD_V	AL2	I	Pr-channel DAC power supply. Connect to a 3.3V nominal supply.
VO2_AVDD_Y	AK2	I	Y-channel DAC power supply. Connect to a 3.3V nominal supply.
VO2_AVSS	AK5	I	Video output analog block ground connection
VO2_AVSS_U	AM3	I	Pb-channel DAC ground connection
VO2_AVSS_V	AL3	I	Pr-channel DAC ground connection
VO2_AVSS_Y	AK3	I	Y-channel DAC ground connection
VO2_RSET	AJ4	0	DAC current set pin. A resistor (140 ohm, 1% tol erance) connected between this pin and the ground sets the full-scale DAC current.

BDP-HD1

Pin Name	Ball ID	Direction	Description
VO2_U	AM1	0	Analog video output. Outputs Pb signal in component YPbPr mode, or B signal in component the RGB mode. Current output, intended to drive 75 ohm doubly-terminated load.
VO2_V	AL1	0	Analog video output. Outputs Pr signal in component YPbPr mode, or R signal in the component RGB mode. Current output, intended to drive 75 ohm doubly-terminated load.
VO2_VREF	AJ5	В	Video DAC current source reference voltage (1.25V nominal)
VO2_Y	AK1	0	Analog video output. Outputs Y (luminance) signal in component YPbPr mode, or G signal in the component RGB mode. Current output, intended to drive 75 ohm doubly-terminated load.

6

7

8

Α

В

С

D

Е

■ VIDEO PROCESSING SUBSYSTEM • HDMI

Pin Function

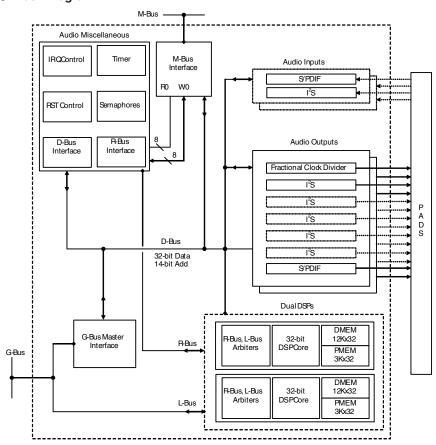
5

5

Pin Name	Ball ID	Direction	Description
HDMI_DSCL	U5	В	HDMI DDC clock
HDMI_DSDA	V5	В	HDMI DDC data (open drain output)
HDMI_HPD	W4	I	HDMI hot plug detect input
HDMI_MSEN	W5	I	HDMI monitor sense
HDMI_PD#	T5	0	HDMI power down (active low)
VO0_P0	W3	0	Bit 0 (LSB) of double-data rate bus to external HDMI PHY device
VO0_P1	V4	0	Bit 1 of double-data rate bus to external HDMI PHY device
VO0_P2	V3	0	Bit 2 of double-data rate bus to external HDMI PHY device
VO0_P3	U4	0	Bit 3 of double-data rate bus to external HDMI PHY device
VO0_P4	U3	0	Bit 4 of double-data rate bus to external HDMI PHY device
VO0_P5	T4	0	Bit 5 of double-data rate bus to external HDMI PHY device
VO0_P6	Т3	0	Bit 6 of double-data rate bus to external HDMI PHY device
VO0_P7	T2	0	Bit 0 of double-data rate bus to external HDMI PHY device
VO0_P8	T1	0	Bit 8 of double-data rate bus to external HDMI PHY device
VO0_P9	R5	0	Bit 9 of double-data rate bus to external HDMI PHY device
VO0_P10	R4	0	Bit 10 of double-data rate bus to external HDMI PHY device
VO0_P11	R3	0	Bit 11 (MSB) of double-data rate bus to external HDMI PHY device
VO0_P12	R2	0	`CTL2 'signal to external HDMI PHY device
VO0_P13	R1	0	`CTL3 'signal to external HDMI PHY device

■ AUDIO PROCESSING SUBSYSTEM

Block Diagram



■ AUDIO PROCESSING SUBSYSTEM

Audio Input Interface

Pin Function

Pin Name	Ball ID	Direction	Description
SI0_BCLK	AN7	I	Audio input 0 serial bit clock = LRCLKx32 / 64. Maximum frequency is 12.288MHz.
SI0_DATA	AP7	I	Audio input 0 serial data
SI0_LRCLK	AL7	I	Audio input 0 serial left/right clock
SI0_SPDIF	AM7	I	Audio input 0 serial data S/PDIF
SI1_BCLK	AL8	I	Audio input 1 serial bit clock = LRCLKx32 / 64. Maximum frequency is 12.288MHz.
SI1_DATA	AM8	I	Audio input 1 serial data
SI1_LRCLK	AK7	I	Audio input 1 serial left/right clock
SI1_SPDIF	AK8	I	Audio input 1 serial data S/PDIF

112

F

В

С

D

Е

BDP-HD1

2

■ AUDIO PROCESSING SUBSYSTEM • Audio Output Interface

● Pin Function

5

5

Pin Name	Ball ID	Direction	Description
SO0_BCLK	AP3	0	Audio output 0 $\rm I^2S$ audio bit clock output, Maximum frequency is 12.288MHz.
SO0_DATA1	AP4	0	Audio output 0 ${ m I}^2{ m S}$ channel 1 audio data output
SO0_DATA2	AN3	0	Audio output 0 I ² S channel 2 audio data output
SO0_DATA3	AN4	0	Audio output 0 $\mathrm{I}^2\mathrm{S}$ channel 3 audio data output
SO0_DATA4	AM4	0	Audio output 0 I ² S channel 4 audio data output
SO0_DATA5	AL4	0	Audio output 0 I ² S channel 5 audio data output
SO0_LRCLK	AN2	0	Audio output 0 I ² S audio frame clock output
SO0_MACLK	AP2	0	Audio output 0 audio clock generator master clock output. Maximum frequency is 50MHz.
SO0_SPDIF	AN1	0	Audio output 0 S/PDIF audio data output
SO1_BCLK	AN5	0	Audio output 1 $\mathrm{I}^2\mathrm{S}$ audio bit clock output. Maximum frequency is 12,288MHz.
SO1_DATA1	AP6	0	Audio output 1 ${ m I}^2{ m S}$ channel 1 audio data output
SO1_DATA2	AM6	0	Audio output 1 I ² S channel 2 audio data output
SO1_DATA3	AN6	0	Audio output 1 I ² S channel 3 audio data output
SO1_DATA4	AL6	0	Audio output 1 $\mathrm{I}^2\mathrm{S}$ channel 4 audio data output
SO1_DATA5	AL5	0	Audio output 1 I ² S channel 5 audio data output
SO1_LRCLK	AK6	0	Audio output 1 I ² S audio frame clock output
SO1_MACLK	AP5	0	Audio output 1 audio clock generator master clock output. Maximum frequency is 50MHz.
SO1_SPDIF	AM5	0	Audio output 1 S/PDIF audio data output

BDP-HD1

8

113

8

Α

В

С

D

Ε

F

■ 2 **■** 3 **■** 4

■ TRANSPORT DEMULTIPLEXER

Block Diagram

Α

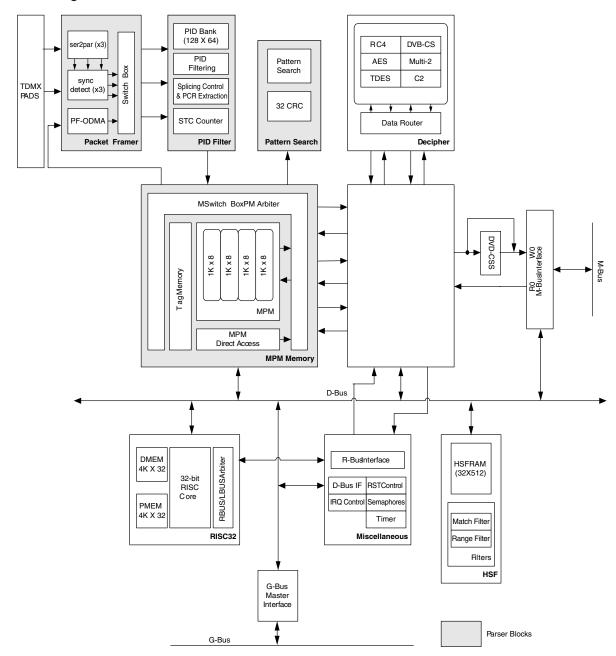
В

С

D

Е

F



■ TRANSPORT DEMULTIPLEXER

• SPI Transport Stream Interface

Pin Function

Pin Name	Ball ID	Direction	Description	
TDMX_GPIO0	AB30	В	Transport demultiplexer GPIO 0	
TDMX_GPIO1	AB31	В	Transport demultiplexer GPIO 1	
TS0_CLK	AF34	I	SPI port clock input data is transferred on the positive-going edge of this clock. When the port is operated in the SSI mode, this pin is not used.	
TS0_IN_D0	AE33	I	SPI input data bit 0 (LSB). When the port is operated in the SSI mode, this pin is the SSI0_DATA input.	
			BDP-HD1	

114

2

3

	6	-	7	8

Pin Name	Ball ID	Direction	Description
TS0_IN_D1	AF33	I	SPI input data bit 1. When the port is operated in the SSI mode, this pin is the SSIO_CLK input.
TS0_IN_D2	AE32	I	SPI input data bit 2. When the port is operated in the SSI mode, this pin is the SSIO_SYNC input.
TS0_IN_D3	AF32	I	SPI input data bit 3. When the port is operated in the SSI mode, this pin is the SSIO_VLD input.
TS0_IN_D4	AE31	I	SPI input data bit 4. When the port is operated in the SSI mode, this pin is the SSI1_DATA input.
TS0_IN_D5	AF31	I	SPI input data bit 5. When the port is operated in the SSI mode, this pin is the SSI1_CLK input.
TS0_IN_D6	AE30	I	SPI input data bit 6. When the port is operated in the SSI mode, this pin is the SSI1_SYNC input.
TS0_IN_D7	AF30	I	SPI input data bit 7 (MSB), When the port is operated in the SSI mode, this pin is the SSI1_VLD input.
TS0_IN_SYNC	AE34	I	SPI sync (selectable polarity, active high/low). Identifies the first byte of a packet. When the port is operated in the SSI mode, this pin is not used.
TS0_IN_VLD	AD30	I	SPI data valid (active high). Indicates valid transport packet bytes. When the port is operated in the SSI mode, this pin is not used.
TS1_CLK	AC34	I	SPI port clock input data is transferred on the positive-going edge of this clock. When the port is operated in the SSI mode, this pin is not used.
TS1_IN_D0	AD34	I	SPI input data bit 0 (LSB). When the port is operated in the SSI mode, this pin is the SSI2_DATA input.
TS1_IN_D1	AB33	I	SPI input data bit 1. When the port is operated in the SSI mode, this pin is the SSI2_CLK input.
TS1_IN_D2	AC33	I	SPI input data bit 2. When the port is operated in the SSI mode, this pin is the SSI2_SYNC input.
TS1_IN_D3	AD33	I	SPI input data bit 3. When the port is operated in the SSI mode, this pin is the SSI2_VLD input.
TS1_IN_D4	AC32	I	SPI input data bit 4.
TS1_IN_D5	AD32	I	SPI input data bit 5.
TS1_IN_D6	AC31	I	SPI input data bit 6.
TS1_IN_D7	AD31	I	SPI input data bit 7 (MSB).
TS1_IN_SYNC	AB32	I	SPI sync (selectable polarity, active high/low). Identifies the first byte of a packet. When the port is operated in the SSI mode, this pin is not used.
TS1_IN_VLD	AC30	I	SPI data valid (active high). Indicates valid transport packet bytes. When the port is operated in the SSI mode, this pin is not used.

■ SHARED PINS • Uart

5

5

Pin Function

Pin Name	Ball ID	Direction	Description	Alternate Function	Alternate Function
UART1_RX	A12	В	UART 1 receive data input	EJ_TDI. Test data input (TDI) for the EJTAG TAP.	GPIO0
UART1_CTS	C12	В	UART 1 clear to send. Flow con- trol signal.	EJ_TMS. Test mode select input (TMS) for the EJTAG TAP.	GPIO1

BDP-HD1

115

Α

В

С

D

Ε

F

2 3

4

4

Alternate Function Alternate Function Pin Name Ball ID Direction Description EJ_TRST_N. Active-low Test Reset Input (TRST) for the EJTAG TAP. At UART 1 data set ready. Data set status signal. GPIO2 UART1_DSR B11 В power-up, the assertion of EJ_TRST_N causes the TAP controller to be reset. EJ_TCK. Test clock input (TCK) for the EJTAG TAP. UART1_DCD C11 В UART 1 data car-GPIO3 rier detect. Data set status signal. UART1_TX A11 В UART 1 transmit GPIO4 data output UART1_RTS B10 В UART 1 request EJ_TDO. Test GPIO5 data output (TDO) for the EJTAG TAP to send. Flow control signal. UART1_DTR C10 В UART 1 data ter-GPI06 minal ready. Data terminal status signal. UART 0 receive data input UARTO_RX GPIO0 A14 В UART 0 clear to send. Flow con-trol signal. UARTO_CTS B14 В GPIO1 UART 0 data set ready. Data set status signal. UARTO_DSR C14 В GPIO2 UARTO_DCD B12 UART 0 data car-rier detect. Data GPIO3 В set status signal. UARTO_TX UART 0 transmit data output A13 В GPIO4 UART 0 request to send. Flow control signal. UARTO_RTS B13 В GPIO5 UART 0 data ter-minal ready. Data terminal status signal. UARTO_DTR C13 GPIO6 В

■ SHARED PINS • GPIO

Pin Function

Α

В

С

D

Ε

F

116

Pin Name	Ball ID	Direction	Alternate Function
GPIO2	C5	В	FIP serial data input
GPIO3	D5	В	FIP serial data output
GPIO4	D4	В	FIP data strobe
GPIO5	E4	В	FIP serial I/O clock
GPIO12	В7	В	Infrared decoder. Default pin assigned to the IR decoder input function (may be mapped to any other GPIO pin under the software control).
GPIO0	A5	В	I2CM_SCL. I ² C master interface serial clock.
GPIO1	B5	В	I2CM_SDA. I ² C master interface serial data.
GPIO6	E5	В	I2CS_SCL. I ² C slave interface serial clock.
GPIO7	В6	В	I2CS_SDA. I ² C slave interface serial data.

BDP-HD1

■ SHARED PINS • Ethernet

5

Pin Function

Pin name	Ball ID	Direction	Alternate Function
GPIO0	AA1	В	ETH_TXCLK. Ethernet transmit clock.
GPIO1	AA2	В	ETH_TX_EN. Ethernet transmit enable.
GPIO2	Y3	В	ETH_TXD0. Ethernet transmit data 0.
GPIO3	Y2	В	ETH_TXD1. Ethernet transmit data 1.
GPIO4	Y1	В	ETH_TXD2. Ethernet transmit data 2.
GPIO5	W1	В	ETH_TXD3. Ethernet transmit data 3.
GPIO6	AC2	В	ETH_RXCLK. Ethernet receive clock.
GPIO7	AE1	В	ETH_RX_DV. Ethernet receive data valid.
GPIO8	AF1	В	ETH_RX_ER. Ethernet receive error.
GPIO9	AC1	В	ETH_RXD0. Ethernet receive data 0.
GPIO10	AB3	В	ETH_RXD1. Ethernet receive data 1.
GPIO11	AB2	В	ETH_RXD2. Ethernet receive data 2.
GPIO12	AB1	В	ETH_RXD3, Ethernet receive data 3.
GPIO13	AA3	В	ETH_CRS. Ethernet carrier sense.
GPIO14	AC3	В	ETH_COL. Ethernet collision detect.
GPIO15	AD1	В	ETH_MDC. Ethernet management data clock.
GPIO16	Y4	В	ETH_MDIO. Ethernet management data I/O.
GPIO17	AA5	В	ETH_MDINT#, Ethernet management interrupt,

■ MISCELLANEOUS PINS

• Miscellaneous

Pin Function

Pin Name	Ball ID	Direction	Description
NC	A1	-	No connect
NC	A34	-	No connect
NC	AA4	-	No connect
NC	AK25	-	No connect
NC	W2	-	No connect
NC	W32	=	No connect
NC	W33	-	No connect
NC	W34	-	No connect
NC	Y5	-	No connect
NC	Y30	=	No connect
NC	Y31	-	No connect
NC	Y32	-	No connect
NC	Y33		No connect
NC	Y34	-	No connect
NC	AA30	-	No connect
NC	AA31	-	No connect

BDP-HD1

117

8

Α

В

С

D

Е

Pin Name	Ball ID	Direction	Description
NC	AA32	-	No connect
NC	AA33	-	No connect
NC	AA34	-	No connect
NC	AB34	-	No connect
NC	AK26	-	No connect
NC	AK27	-	No connect
NC	AK28	-	No connect
NC	AL26	-	No connect
NC	AM26	-	No connect
NC	AN26	-	No connect
NC	AP1	-	No connect
NC	AP26	-	No connect
NC	AP34	-	No connect
RESET#	A8	I	Device reset input. Active low.
RTC_TEST	W3	I	Used for manufacturing purposes only
TEST	E10	I	Test mode input. Tie to VSS for normal operation.
XTAL_DISC	E11	I	Used for manufacturing purposes only

■ LISTING OF GROUND PINS (VSS)

• Ground

С

D

Ε

Pin Function

Pin Name	Ball ID	Direction	Description
VSS	F6	I	Ground. Zero volt reference for 1.2, 2.5 and 3.3V supplies
VSS	F8	I	Ground
VSS	F11	I	Ground
VSS	F12	I	Ground
VSS	F15	I	Ground
VSS	F16	I	Ground
VSS	F19	I	Ground
VSS	F20	I	Ground
VSS	F21	I	Ground
VSS	F24	I	Ground
VSS	F26	I	Ground
VSS	G7	I	Ground
VSS	G9	Ī	Ground
VSS	G10	I	Ground
VSS	G13	I	Ground
VSS	G14	I	Ground
VSS	G17	I	Ground
VSS	G18	I	Ground
VSS	G22	I	Ground
VSS	G25	I	Ground

8

BDP-HD1

Ball ID Pin Name Direction Description VSS G26 Ι Ground I VSS G28 Ground VSS Ι Н6 Ground VSS J7 I Ground VSS I J28 Ground I VSS J29 Ground VSS Κ7 Ι Ground VSS K28 I Ground VSS L6 Ι Ground VSS М6 I Ground I VSS N7 Ground VSS N28 I Ground VSS N29 I Ground VSS Р7 I Ground I VSS P14 Ground I VSS P15 Ground VSS P16 I Ground VSS P17 I Ground VSS P18 Ι Ground VSS P19 I Ground VSS P20 Ι Ground I VSS P21 Ground I VSS P28 Ground I VSS R6 Ground VSS R14 I Ground VSS R15 Ι Ground VSS R16 I Ground VSS R17 I Ground VSS R18 I Ground VSS R19 I Ground VSS R20 I Ground I VSS R21 Ground I VSS R29 Ground I VSS Т6 Ground I VSS T14 Ground VSS T15 I Ground I VSS T16 Ground VSS T17 I Ground VSS T18 Ι Ground VSS T19 I Ground VSS T20 Ι Ground T21 I VSS Ground VSS U7 Ι Ground

6

7

Α

8

В

С

D

Ε

_

F

6

8

1 2 3 4

Pin Name	Ball ID	Direction	Description	Pin Name	Ba	ll ID
S	U14	I	Ground	VSS	AA16	
S	U15	I	Ground	VSS	AA17	
/SS	U16	I	Ground	VSS	AA18	
SS	U17	I	Ground	VSS	AA19	
S	U18	I	Ground	VSS	AA20	
iS	U19	I	Ground	VSS	AA21	
S	U20	I	Ground	VSS	AA28	
S	U21	I	Ground	VSS	AB7	
5	U28	I	Ground	VSS	AB28	
5	V7	I	Ground	VSS	AC6	
SS	V14	I	Ground	VSS	AC29	
S	V15	I	Ground	VSS	AD6	
S	V16	I	Ground	VSS	AD29	-
SS	V17	I	Ground	VSS	AE7	
SS	V18	I	Ground	VSS	AE28	
S	V19	I	Ground	VSS	AF7	
S	V20	I	Ground		AF28	
S	V21	I	Ground	VSS	AG6	
SS	V28	I	Ground	VSS	AG29	_
S	V29	I	Ground	VSS	AH6	
S	W6	I	Ground	VSS	AH7	
5	W14	I	Ground		AH9	
s	W15	I	Ground		AH10	
5	W16	I	Ground		AH13	
	W17	I	Ground		AH14	
S S	W17	I	Ground			
				VSS	AH17	
SS	W19	I	Ground	VSS	AH18	
S 	W20	I	Ground	VSS	AH21	
S 	W21	I	Ground	VSS	AH22	
5	W29	I	Ground	VSS	AH25	
	Y6	I	Ground	VSS	AH26	
-	Y14	I	Ground	VSS	AH28	
SS	Y15	I	Ground	VSS	AJ6	
S	Y16	I	Ground	VSS	АЈ7	
SS	Y17	I	Ground	VSS	AJ8	
SS	Y18	I	Ground	VSS	AJ11	
SS	Y19	I	Ground	VSS	AJ12	
S	Y20	I	Ground	VSS	AJ15	
S	Y21	I	Ground	VSS	AJ16	
S	Y29	I	Ground	VSS	AJ19	
SS	AA7	I	Ground	VSS	AJ20	
SS	AA14	I	Ground	VSS	AJ23	
/SS	AA15	I	Ground	VSS	AJ24	

BDP-HD1
1 ■ 2 ■

В

С

D

Ε

Pin Name	Ball ID	Direction	Description
VSS	AJ27	I	Ground
VSS	AJ29	I	Ground
VSS_PLL3	E12	I	Ground, Dedicated connection for PLL#3
VSS_PLL2	E13	I	Ground. Dedicated connection for PLL#2
VSS_PLL1	E14	I	Ground. Dedicated connection for PLL#1
VSS_PLL0	E15	I	Ground. Dedicated connection for PLL#0

■ VOLT POWER RAIL

• 1.2V Power Rail (VDD_1V2)

Pin Function

Pin Name	Ball ID	Direction	Description
VDD_1V2	G8	I	1.2V (nominal) power supply
VDD_1V2	G11	I	1.2V (nominal) power supply
VDD_1V2	G12	I	1.2V (nominal) power supply
VDD_1V2	G15	I	1.2V (nominal) power supply
VDD_1V2	G16	I	1.2V (nominal) power supply
VDD_1V2	G19	I	1.2V (nominal) power supply
VDD_1V2	G20	I	1.2V (nominal) power supply
VDD_1V2	G21	I	1.2V (nominal) power supply
VDD_1V2	G23	I	1.2V (nominal) power supply
VDD_1V2	G24	I	1.2V (nominal) power supply
VDD_1V2	G27	I	1.2V (nominal) power supply
VDD_1V2	H7	I	1.2V (nominal) power supply
VDD_1V2	H28	I	1.2V (nominal) power supply
VDD_1V2	L7	I	1.2V (nominal) power supply
VDD_1V2	L28	I	1.2V (nominal) power supply
VDD_1V2	M7	I	1.2V (nominal) power supply
VDD_1V2	M28	I	1.2V (nominal) power supply
VDD_1V2	R7	I	1.2V (nominal) power supply
VDD_1V2	R28	I	1.2V (nominal) power supply
VDD_1V2	T7	I	1.2V (nominal) power supply
VDD_1V2	T28	I	1.2V (nominal) power supply
VDD_1V2	W7	I	1.2V (nominal) power supply
VDD_1V2	W28	I	1.2V (nominal) power supply
VDD_1V2	Y7	I	1.2V (nominal) power supply
VDD_1V2	Y28	I	1.2V (nominal) power supply
VDD_1V2	AC7	I	1.2V (nominal) power supply
VDD_1V2	AC28	I	1.2V (nominal) power supply
VDD_1V2	AD7	I	1.2V (nominal) power supply
VDD_1V2	AD28	I	1.2V (nominal) power supply
VDD_1V2	AG7	I	1.2V (nominal) power supply
VDD_1V2	AG28	I	1.2V (nominal) power supply

В

D

Е

■ 2 ■ 3 ■ 4

Pin Name	Ball ID	Direction	Description
VDD_1V2	AH8	I	1.2V (nominal) power supply
VDD_1V2	AH11	I	1.2V (nominal) power supply
VDD_1V2	AH12	I	1.2V (nominal) power supply
VDD_1V2	AH15	I	1.2V (nominal) power supply
VDD_1V2	AH16	I	1.2V (nominal) power supply
VDD_1V2	AH19	I	1.2V (nominal) power supply
VDD_1V2	AH20	I	1.2V (nominal) power supply
VDD_1V2	AH23	I	1.2V (nominal) power supply
VDD_1V2	AH24	I	1.2V (nominal) power supply
VDD_1V2	AH27	I	1.2V (nominal) power supply
VDD_PLL0_1V2	D12	I	1.2V (nominal) power supply. Dedicated power connection for PLL#0.

■ VOLT POWER RAIL

• 2.5V Power Rail (VDD_2V5)

Pin Function

Pin Name	Ball ID	Direction	Description
VDD_2V5	F22	I	2.5/2.6V (nominal) power supply
VDD_2V5	F23	I	2.5/2.6V (nominal) power supply
VDD_2V5	F25	I	2.5/2.6V (nominal) power supply
VDD_2V5	F27	I	2.5/2.6V (nominal) power supply
VDD_2V5	F29	I	2.5/2.6V (nominal) power supply
VDD_2V5	H29	I	2.5/2.6V (nominal) power supply
VDD_2V5	K29	I	2.5/2.6V (nominal) power supply
VDD_2V5	M29	I	2.5/2.6V (nominal) power supply
VDD_2V5	P29	I	2.5/2.6V (nominal) power supply
VDD_2V5	T29	I	2.5/2.6V (nominal) power supply
VDD_2V5	U29	I	2.5/2.6V (nominal) power supply

■ VOLT POWER RAIL

• 3.3V Power Rail (VDD_3V3)

Pin Function

Pin Name	Ball ID	Direction	Description
VDD_3V3	F7	I	3.3V (nominal) power supply
VDD_3V3	F9	I	3.3V (nominal) power supply
VDD_3V3	F10	I	3.3V (nominal) power supply
VDD 3V3	F13	I	2.21/ (nominal) newer cumby
VDD_3V3	F13	1	3.3V (nominal) power supply
VDD 3V3	F14	I	3.3V (nominal) power supply
VDD_3V3	F17	I	3.3V (nominal) power supply
VDD_3V3	F18	I	3.3V (nominal) power supply
VDD_3V3	G6	I	3.3V (nominal) power supply

122

D

Ε

F

2

BDP-HD1

3

Pin Name	Ball ID	Direction	Description
VDD_3V3	J6	I	3.3V (nominal) power supply
VDD_3V3	K6	I	3.3V (nominal) power supply
VDD_3V3	N6	Ī	3.3V (nominal) power supply
VDD_3V3	P6	I	3.3V (nominal) power supply
VDD_3V3	U6	I	3.3V (nominal) power supply
VDD_3V3	V6	I	3.3V (nominal) power supply
VDD_3V3	AA6	I	3.3V (nominal) power supply
VDD_3V3	AA29	Ī	3.3V (nominal) power supply
VDD_3V3	AB6	I	3.3V (nominal) power supply
VDD_3V3	AB29	Ī	3.3V (nominal) power supply
VDD_3V3	AE6	I	3.3V (nominal) power supply
VDD_3V3	AE29	I	3.3V (nominal) power supply
VDD_3V3	AF6	I	3.3V (nominal) power supply
VDD_3V3	AF29	I	3.3V (nominal) power supply
VDD_3V3	AH29	I	3.3V (nominal) power supply
VDD_3V3	AJ9	I	3.3V (nominal) power supply
VDD_3V3	AJ10	I	3.3V (nominal) power supply
VDD_3V3	AJ13	I	3.3V (nominal) power supply
VDD_3V3	AJ14	I	3.3V (nominal) power supply
VDD_3V3	AJ17	I	3.3V (nominal) power supply
VDD_3V3	AJ18	I	3.3V (nominal) power supply
VDD_3V3	AJ21	I	3.3V (nominal) power supply
VDD_3V3	AJ22	I	3.3V (nominal) power supply
VDD_3V3	AJ25	I	3.3V (nominal) power supply
VDD_3V3	AJ26	I	3.3V (nominal) power supply
VDD_3V3	AJ28	I	3.3V (nominal) power supply
VDD_PLL1_3V3	D13	I	3.3V (nominal) power supply Dedicated power connection for PLL#1.
VDD_PLL2_3V3	D14	I	3.3V (nominal) power supply. Dedicated power connection for PLL#2.
VDD_PLL3_3V3	D15	I	3.3V (nominal) power supply. Dedicated power connection for PLL#3.

6

7

8

В

С

_

D

Ε

F

8

1 2 3 4

■ PIN ARRANGEMENT

■ Top Left Quadrant

Α

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	NC	VI1_ P0	VI1_ CLK	VI1_ VS	GPIO0	RCLK1_ XTAL_ OUT	RCLK1_ XTAL_IN	RESET#	XTAL_ OUT	XTAL_ IN	UART1_ TX	UART1_ RX	UART0_ TX	UART0_ RX	SCARD_ IO	SCARD_ CLK	IDE_ D6
В	VI1_ P4	VI1_ P1	VI1_ HS	VI1_ VLD	GPIO1	GPI07	GPIO12	RCLK0_ IN	XTAL_ BUF	UART1_ RTS	UART1_ DSR	UART0_ DCD	UART0_ RTS	UART0_ CTS	SCARD_ RST	SCARD_ FC#	IDE_ D10
С	VI1_ P5	VI1_ P6	VI1_ P2	VI1_ P3	GPIO2	GPIO8	GPIO13	VCXO1_ IN	VCXO0_ IN	UART1_ DTR	UART1_ DCD	UART1_ CTS	UART0_ DTR	UART0_ DSR	SCARD_ CTL0	IDE_ D8	IDE_ D5
D	VI0_ P1	VI0_ P0	VI1_ P7	GPIO4	GPIO3	GPIO9	GPIO14	RCLK0_ OUT	RCLK1_ OUT	RCLK2_ OUT	T AG_ UART#	VDD_ PLL0_ 1V2	VDD_ PLL1_ 3V3	VDD_ PLL2_ 3V3	VDD_ PLL3_ 3V3	SCARD_ CTL1	IDE_ D7
E	VI0_ P4	VI0_ P3	VI0_ P2	GPIO5	GPIO6	GPIO10	GPIO15	GPIO11	RCLK3_ OUT	TEST	XTAL_ DISC	VSS_ PLL0	VSS_ PLL1	VSS_ PLL2	VSS_ PLL3	SCARD_ CTL2	IDE_ D9
F	VI0_ P9	VIO_ P8	VI0_ P7	VI0_ P6	VI0_ P5	VSS	VDD_3V3	VSS	VDD_3V3	VDD_3V3	VSS	VSS	VDD_3V3	VDD_3V3	VSS	VSS	VDD_3V3
G	VI0_ P14	VI0_ P13	VI0_ P12	VI0_ P11	VI0_ P10	VDD_3V3	VSS	VDD_1V2	VSS	VSS	VDD_1V2	VDD_1V2	VSS	VSS	VDD_1V2	VDD_1V2	vss
н	VI0_ P19	VI0_ P18	VI0_ P17	VI0_ P16	VI0_ P15	VSS	VDD_1V2										
	VIO_ VS	VIO_ HS	VI0_ P22	VI0_ P21	VI0_ P20	VDD_3V3	VSS										
к	VIO_ CLK	VIO_ VLD	VI0_ P25	VI0_ P24	VI0_ P23	VDD_3V3	VSS										
L	VI2_ VS	VI2_ HS	VI0_ P28	VI0_ P27	VI0_ P26	VSS	VDD_1V2										
М	VI2_ CLK	VI2_ VLD	VI0_ P31	VI0_ P30	VI0_ P29	VSS	VDD_1V2										
N	VO0_ P23	VO0_ P22	VO0_ P21	VO0_ P20	VO0_ P19	VDD_3V3	VSS										
Р	VO0_ P18	VO0_ P17	VO0_ P16	VO0_ P15	VO0_ P14	VDD_3V3	VSS							VSS	VSS	VSS	vss
R	VO0_ P13	VO0_ P12	VO0_ P11	VO0_ P10	VO0_ P9	VSS	VDD_1V2							VSS	VSS	VSS	vss
т	VO0_ P8	VO0_ P7	VO0_ P6	VO0_ P5	HDMI_ PD#	VSS	VDD_1V2							VSS	VSS	VSS	vss
U	VO0_ CLK	VO0_ VLD	VO0_ P4	VO0_ P3	HDMI_ DSCL	VDD_3V3	vss							VSS	VSS	VSS	vss

F

D

Ε

1 ■ 2 ■ 3 ■ 4

■ 6 **■** 7 **■** 8

● Top Right Quadrant

VSS

VSS

VSS

vss

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
IDE_ D12	IDE_ D1	IDE_ IOR#	IDE_ NPCBLID	DRAM1_ DQ13	DRAM1_ DQ9	DRAM1_ DQS0	DRAM1_ DQ4	DRAM1_ CK	DRAM1_ CK#	DRAM1_ DQ27	DRAM1_ DM3	DRAM1_ DQ21	DRAM1_ DQ16	DRAM1_ CAS#	DRAM1_ BA0	NC	А
IDE_ D3	IDE_ D15	IDE_ IORDY	IDE_ A0	DRAM1_ DQ14	DRAM1_ DQ10	DRAM1_ DM0	DRAM1_ DQ5	DRAM1_ DQ2	DRAM1_ DQ31	DRAM1_ DQ26	DRAM1_ DM2	DRAM1_ DQ20	DRAM1_ A13	DRAM1_ RAS#	DRAM1_ BA1	DRAM1_ A0	В
IDE_ D13	IDE_ D0	IDE_ ACK#	IDE_ A2	DRAM1_ DQ15	DRAM1_ DQ11	DRAM1_ DM1	DRAM1_ DQ6	DRAM1_ DQ3	DRAM1_ DQ30	DRAM1_ DQ25	DRAM1_ DQS2	DRAM1_ DQ19	DRAM1_ WE#	DRAM1_ CS#	DRAM1_ A10	DRAM1_ A1	С
IDE_ D11	IDE_ D2	IDE_ DMARQ	IDE_ IRQ	IDE_ CS0#	DRAM1_ DQ12	DRAM1_ DQ8	DRAM1_ DQ7	DRAM1_ DQ0	DRAM1_ DQ28	DRAM1_ DQS3	DRAM1_ DQ22	DRAM1_ DQ17	DRAM1_ A9	DRAM1_ A6	DRAM1_ A4	DRAM1_ A2	D
IDE_ D4	IDE_ D14	IDE_ IOW#	IDE_ A1	IDE_ CS1#	DRAM1_ VREFSS TL2	DRAM1_ DQS1	DRAM1_ VREFSS TL1	DRAM1_ DQ1	DRAM1_ DQ29	DRAM1_ DQ24	DRAM1_ DQ23	DRAM1_ DQ18	DRAM1_ A11	DRAM1_ A7	DRAM1_ A5	DRAM1_ A3	E
VDD_3V3	3 VSS	VSS	vss	VDD_2V5	VDD_2V5	VSS	VDD_2V5	VSS	VDD_2V5	DRAM1_ VREFSS TL0	VDD_2V5	DRAM1_ CKE	DRAM1_ A12	DRAM1_ A8	DRAM0_ DQ15	DRAM0_ DQ14	F
VSS	VDD_1V2	VDD_1V2	VDD_1V2	VSS	VDD_1V2	VDD_1V2	VSS	VSS	VDD_1V2	VSS	DRAM0_ VREFSS TL2	DRAM0_ DQ12	DRAM0_ DQ13	DRAM0_ DQ11	DRAM0_ DQ10	DRAM0_ DQ9	G
										VDD_1V2	VDD_2V5	DRAM0_ DQS1	DRAM0_ DQ8	DRAM0_ DM1	DRAMO_ DMO	DRAM0_ DQS0	
										VSS	VSS	DRAM0_ VREFSS TL1	DRAM0_ DQ7	DRAM0_ DQ6	DRAM0_ DQ5	DRAM0_ DQ4	
										VSS	VDD_2V5	DRAM0_ DQ1	DRAM0_ DQ0	DRAM0_ DQ3	DRAM0_ DQ2	DRAM0_ CK	к
										VDD_1V2	DRAMO_ VREFSS TL0	DRAM0_ DQ29	DRAM0_ DQ28	DRAM0_ DQ30	DRAM0_ DQ31	DRAM0_ CK#	L
										VDD_1V2	VDD_2V5	DRAM0_ DQ24	DRAM0_ DQS3	DRAM0_ DQ25	DRAM0_ DQ26	DRAM0_ DQ27	М
										VSS	VSS	DRAM0_ DQ23	DRAM0_ DQ22	DRAM0_ DQS2	DRAM0_ DM2	DRAMO_ DM3	N
vss	VSS	VSS	VSS							vss	VDD_2V5	DRAM0_ DQ18	DRAM0_ DQ17	DRAM0_ DQ19	DRAM0_ DQ20	DRAM0_ DQ21	Р
VSS	VSS	VSS	VSS							VDD_1V2	VSS	DRAM0_ CKE	DRAM0_ A12	DRAM0_ WE#	DRAM0_ A13	DRAM0_ DQ16	R
VSS	VSS	VSS	VSS							VDD_1V2	VDD_2V5	DRAM0_ A11	DRAM0_ A9	DRAM0_ CS#	DRAM0_ RAS#	DRAM0_ CAS#	т

В

D

Ε

125

■ 7

1 2 3 4

Bottom Left Quadrant

В

С

D

Е

	VO0_	VO0_	VO0_	VO0_	HDMI_												
V	HS	VS	P2	P1	DSDA	VDD_3V3	VSS							VSS	VSS	VSS	VSS
w	ETH_ TXD3	NC	VO0_ P0	HDMI_ HPD	HDMI_ MSEN	VSS	VDD_1V2							VSS	vss	vss	VSS
Υ	ETH_ TXD2	ETH_ TXD1	ETH_ TXD0	ETH_ MDIO	NC	VSS	VDD_1V2							VSS	VSS	VSS	VSS
AA	ETH_ TXCLK	ETH_ TX_ EN	ETH_ CRS	NC	ETH_ MDINT#	VDD_3V3	VSS							VSS	VSS	VSS	VSS
АВ	ETH_ RXD3	ETH_ RXD2	ETH_ RXD1	GPIO31	GPIO30	VDD_3V3	VSS										
AC	ETH_ RXD0	ETH_ RXCLK	ETH_ COL	GPIO29	GPIO28	VSS	VDD_1V2										
AD	ETH_ MDC	GPIO27	GPIO26	GPIO25	GPIO24	VSS	VDD_1V2										
ΑE	ETH_ RX_ DV	GPIO23	GPIO22	GPIO21	GPIO20	VDD_3V3	VSS										
AF	ETH_ RX_ ER	GPIO19	GPIO18	GPIO17	GPIO16	VDD_3V3	VSS										
AG	VO1_ Y	VO1_ AVDD_ Y	VO1_ AVSS_ Y	VO1_ AVDD	VO1_ AVSS	VSS	VDD_1V2										
АН	VO1_ V	VO1_ AVDD_ V	VO1_ AVSS_ V	VO1_ RSET	VO1_ VREF	VSS	VSS	VDD_1V2	VSS	VSS	VDD_1V2	VDD_1V2	VSS	VSS	VDD_1V2	VDD_1V2	VSS
AJ	VO1_ U	VO1_ AVDD_ U	VO1_ AVSS_ U	VO2_ RSET	VO2_ VREF	VSS	VSS	VSS	VDD_3V3	VDD_3V3	VSS	VSS	VDD_3V3	VDD_3V3	vss	vss	VDD_3V3
AK	VO2_ Y	VO2_ AVDD_ Y	VO2_ AVSS_ Y	VO2_ AVDD	VO2_ AVSS	SO1_ LRCLK	SI1_ LRCLK	SI1_ SPDIF	PCI_ REQ1#	PCI_ REQ2#	PCI_ REQ3#	PCI_ IDSEL2	PCI_ IDSEL3	PCI_ AD18	PCI_ AD16	PCI_ AD15	PCI_ AD4
AL	VO2_ V	VO2_ AVDD_ V	VO2_ AVSS_ V	SO0_ DATA5	SO1_ DATA5	SO1_ DATA4	SIO_ LRCLK	SI1_ BCLK	PCI_ REQ0# G NT#	PCI_ AD28	PCI_ AD24	PCI_ IDSEL1	PCI_ AD20	PCI_ FRAME#	PCI_ TRDY#	PCI_ AD13	PCI_ AD11
AM	VO2_ U	VO2_ AVDD_ U	VO2_ AVSS_ U	SO0_ DATA4	SO1_ SPDIF	SO1_ DATA2	SIO_ SPDIF	SI1_ DATA	PCI_ GNT3#	PCI_ GNT2#	PCI_ AD30	PCI_ AD26	PCI_ IDSEL0	PCI_ AD22	PCI_ IRDY#	PCI_ PAR	PCI_ AD12
AN	SO0_ SPDIF	SO0_ LRCLK	SO0_ DATA2	SO0_ DATA3	SO1_ BCLK	SO1_ DATA3	SIO_ BCLK	PCI_ INTA#	PCI_ GNT1#	PCI_ AD29	PCI_ AD25	PCI_ AD23	PCI_ AD21	PCI_ CBE2#	PCI_ STOP#	PCI_ AD14	PCI_ AD10
AP	NC	SOO_ MCLK	SO0_ BCLK	SO0_ DATA1	SO1_ MCLK	SO1_ DATA1	SIO_ DATA	PCI_ CLK	PCI_ GNT0# R EQ#	PCI_ AD31	PCI_ AD27	PCI_ CBE3#	PCI_ AD19	PCI_ AD17	PCI_ DEVSEL #	PCI_ CBE1#	PCI_ AD8
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

126 BDP-HD1 3 = 3

Bottom Right Quadrant

5

VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS

VSS

VDD_1V2 VDD_1V2

VSS

VSS

VDD_1V2 VDD_1V2

VSS

	VSS	VSS	DRAMO_ A6	DRAM0_ A5	DRAM0_ A2	DRAM0_ A1	DRAMO_ A0	v
	VDD_1V2	vss	DRAMO_ A4	DRAM0_ A3	NC	NC	NC	w
	VDD_1V2	VSS	NC	NC	NC	NC	NC	Υ
	vss	VDD_3V3	NC	NC	NC	NC	NC	АА
	VSS	VDD_3V3	TDMX_ GPIO0	TDMX_ GPIO1	TS1_ IN_ SYNC	TS1_ IN_ D1	NC	АВ
	VDD_1V2	VSS	TS1_ IN_ VLD	TS1_ IN_ D6	TS1_ IN_ D4	TS1_ IN_ D2	TS1_ CLK	AC
	VDD_1V2	VSS	TS0_ IN_ VLD	TS1_ IN_ D7	TS1_ IN_ D5	TS1_ IN_ D3	TS1_ IN_ D0	AD
	VSS	VDD_3V3	TS0_ IN_ D6	TS0_ IN_ D4	TS0_ IN_ D2	TSO_ IN_ DO	TS0_ IN_ SYNC	AE
	VSS	VDD_3V3	TS0_ IN_ D7	TS0_ IN_ D5	TS0_ IN_ D3	TS0_ IN_ D1	TS0_ CLK	AF
	VDD_1V2	VSS	PB_ ALE	PB_ CS3#	PB_ CS2#	PB_ CS1#	PB_ CS0#	AG
V2	VSS	VDD_3V3	PB_ DIR#	PB_ AD11	PB_ AD10	PB_ AD	PB_ AD	A
	VDD_3V3	VSS	PB_ A6	PB_ AD15	PB_ AD14	PB_ AD13	PB_ AD12	A
	NC	PB_ A12	PB_ A7	PB_ AD3	PB_ AD2	PB_ AD1	PB_ AD0	AK
	PB_ A17	PB_ A13	PB_ A	PB_ AD7	PB_ AD6	PB_ AD5	PB_ AD4	AL
	PB_ A1	PB_ A14	PB_ A	PB_ A3	PB_ A0	PB_ DMAACK #	PB_ RD#	АМ
	PB_ A1	PB_ A15	PB_ A10	PB_ A4	PB_ A1	PB_ DMARQ	PB_ WR#	AN

7

8

Α

В

С

D

Ε

ΑP

6

VSS VDD_3V3 VDD_3V3 VSS VDD_3V3 VSS VDD_3V3 VDD_3V3 VSS VSS S B20_ SB2 0_ SB2 0_ S B20 PCI_ PCI RTC_ VSSAT VSSAT VSSAT VSSAT NC NC NC AD6 AD2 0 0 RTC RTC S B20_ SB2 0_ S B20 VDD PB PCI PCI SB2 0 VDD VSSAT VDDAC_ VSSAT_ NC AD0 VSSAC BAT_ BAT_ A21 CBE0# 0 3V3 1 3V3 3V3 SB2 0 S B20_ SB2 0_ S B20 PCI_ PCI_ RTC_ RTC_ PB_ VDDAT VDDAT VDDAT_ NC VDDAT_ AD3 RING TEST A22 AD 0_3V3 0_3V3 1_3V3 1_3V3 SB 20_ SB2 0_ RTC_ RTC_ PCI_ PCI_ S B20 S B20 PB_ PB_ PB_ PB_ PB_ PB_ PB_ CLK NC XTAL DP DP_ DMARQ AD7 AD1 REXT **ATEST** A23 **A**1 A15 A10 **A**4 **A**1 WR# DISC 0 IN SB 20_ SB 20 RTC_ RTC_ RTC_ SB2 0_ PB_ PCI_ S B20_ PB_ PB_ PB_ PB_ PB_ PB_ DM_ DM_ CLK_ XTAL_ XTAL_ NC A20 A2 IORDY AD5 ХО ΧI A24 A16 A11 **A5** IN ОТ 0 1 ОТ 1 1 20 21 22 23 24 25 26 27 2 30 31 32 33 34

VSS

VDD_1V

127

8

5

6

6

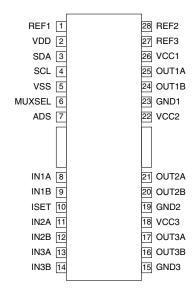
BDP-HD1

1 2 3 4

■ SM5302AS (IC4201)

• HD VIDEO AMP

Pin Arrangement (Top view)



Block Diagram

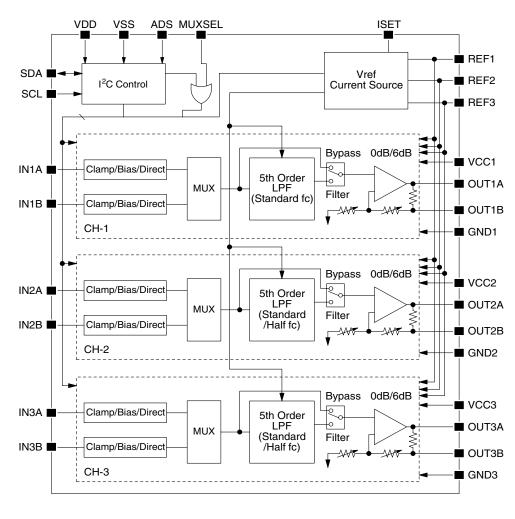
В

С

D

Ε

F



128

— 3

BDP-HD1

• Pin Function

5

No.	Pin Name	I/O *1	A/D *2	Pin Function
1	REF1	0	Α	Internal reference voltage 1
2	VDD	-	D	Digital power supply (3.0 V to 5.5 V)
3	SDA	I/O	D	I2C data signal input/output
4	SCL	I	D	I2C clock signal input
5	VSS	-	D	Digital ground
6	MUXSEL	I	D	Input multiplexer switching pin
7	ADS	I	D	I2C slave address setting pin (3 state)
8	IN1A	I	Α	Video signal input (CH-1, A input)
9	IN1B	I	Α	Video signal input (CH-1, B input)
10	ISET	-	Α	Resistor connection pin for internal current setting (RISET normal 1.8k ohm)
11	IN2A	I	Α	Video signal input (CH-2, A input)
12	IN2B	I	Α	Video signal input (CH-2, B input)
13	IN3A	I	Α	Video signal input (CH-3, A input)
14	IN3B	1	Α	Video signal input (CH-3, B input)
15	GND3	-	Α	Analog ground (CH-3)
16	OUT3B	0	Α	Video signal output (CH-3, for Sag correction)
17	OUT3A	0	Α	Video signal output (CH-3)
18	VCC3	-	Α	Analog power supply (CH-3) (4.75 V to 5.25 V)
19	GND2	-	Α	Analog ground (CH-2)
20	OUT2B	0	Α	Video signal output (CH-2, for Sag correction)
21	OUT2A	0	Α	Video signal output (CH-2)
22	VCC2	-	Α	Analog power supply (CH-2) (4.75 V to 5.25 V)
23	GND1	-	Α	Analog ground (CH-1, Vref)
24	OUT1B	0	Α	Video signal output (CH-1, for Sag correction)
25	OUT1A	0	Α	Video signal output (CH-1)
26	VCC1	_	Α	Analog power supply (CH-1, Vref) (4.75 V to 5.25 V)
27	REF3	0	Α	Internal reference voltage 3
28	REF2	0	Α	Internal reference voltage 2

7

6

*1: I: Input, O: Output *2: A: Analog, D: Digital

5

BDP-HD1

Α

8

В

С

D

Е

F

129

■ K4H510838C (IC2001, 2021, 2901, 2921)

2

3

DDR MEMORY

В

С

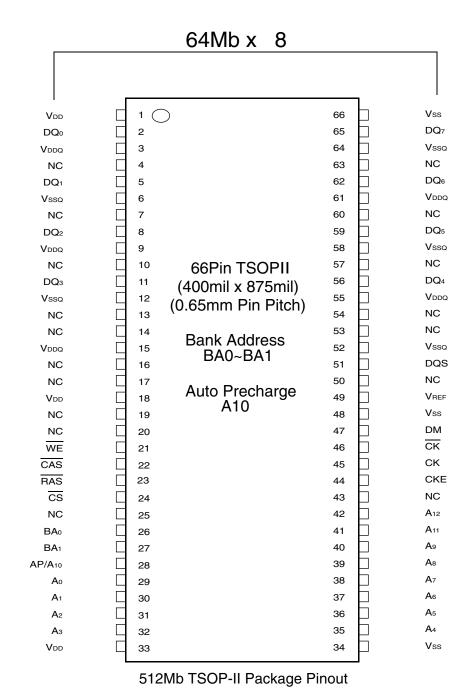
D

Ε

F

130

• Pin Arrangement (Top view)



BDP-HD1

■ 2 ■ 3

■ K4H511638C (IC2101, 2121)

6

7

8

Α

В

D

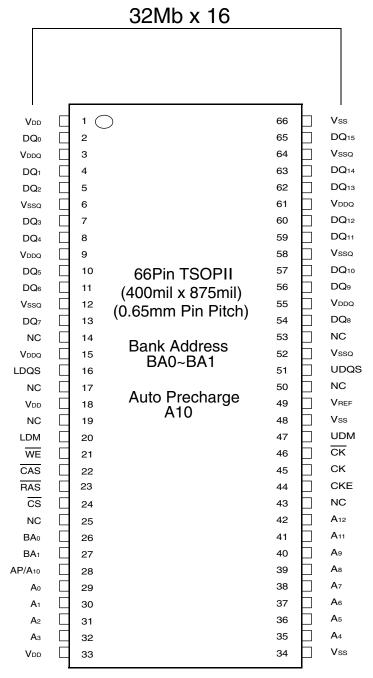
Ε

• DDR MEMORY 32x16

5

5

Pin Arrangement (Top view)



512Mb TSOP-II Package Pinout

BDP-HD1

Α

В

С

D

Е

F

2

3

132

BDP-HD1

.

• Pin Function

5

SYMBOL	TYPE	DESCRIPTION
CK, CK	Input	Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of \overline{CK} . Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/ \overline{CK} .
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE Low provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughput READ and WRITE accesses. Input buffers, excluding CK, CK and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS Low level after Vdd is applied upon 1st power up, After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH entry and exit, VREF must be maintained to this input.
CS	Input	Chip Select: $\overline{\text{CS}}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.
RAS, CAS, WE	Input	Command Inputs : RAS, CAS and WE (along with CS) define the command being entered.
LDM,(UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0~D7; UDM corresponds to the data on DQ8~DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Addres Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied.
A [0 : 12]	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0~D7; UDQS corresponds to the data on DQ8~DQ15
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : +2.5V ± 0.2V. (+2.6V ±0.1V for DDR400)
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : +2.5V ± 0.2V. (+2.6V ±0.1V for DDR400)
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

7 - 8

8

Α

В

С

D

Е

133

_

5

■ PCM1738EG-3 (IC3001, 3401, 3501)

• DIGITAL-TO-ANALOG CONVERTER

Pin Arrangement (Top view)

Α

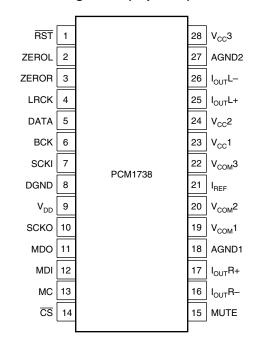
В

С

D

Ε

F



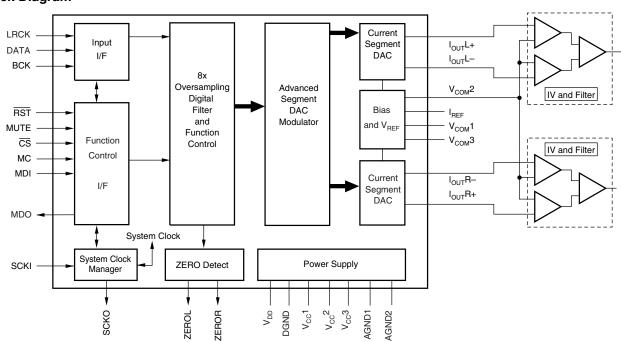
• Pin Function

3

PIN	NAME	TYPE	FUNCTION
1	RST	IN	Reset ⁽¹⁾
2	ZEROL	OUT	Zero Flag for L-Channel.
3	ZEROR	OUT	Zero Flag for R-Channel.
4	LRCK	IN	Left/Right clock (f _S) input for normal operation. (1)
			WDCK clock input in external DF mode. Con-
			nected to GND in DSD mode.
5	DATA	IN	Serial Audio data input for normal operation.(1)
			L-channel audio data input for external DF and
			DSD modes.
6	BCK	IN	Bit Clock. Input. Connected to GND for DSD mode. (1)
7	SCKI	IN	System Clock Input for normal operation.(1)
			BCK (64f _S) clock input for DSD mode.
8	DGND	_	Digital Ground
9	V_{DD}	_	Digital Supply, +3.3V
10	SCKO	OUT	System Clock Output
11	MDO	OUT	Serial data output for function control register. (2)
12	MDI	IN	Serial data input for function control register.(1)
13	MC	IN	Shift Clock for function control register. (1)
14	CS	IN	Mode Control chip select and latch signal. (1)
15	MUTE	IN	Analog output mute control for normal operation.(1)
			R-channel audio data input for external DF and
			DSD modes.
16	I _{OUT} R-	OUT	R-Channel Analog Current Output –
17	I _{OUT} R+	OUT	R-Channel Analog Current Output +
18	AGND1	_	Analog Ground
19	V _{COM} 1	-	Internal Bias Decoupling Pin
20	V _{COM} 2	-	Common Voltage for I/V
21	I _{REF}	-	Output current reference bias pin. Connect 16k
			resistor to GND.
22	V _{COM} 3	_	Internal Bias Decoupling Pin
23	V _{CC} 1	_	Analog Supply, +5.0V
24	V _{CC} 2		Analog Supply, +5.0V
25	I _{OUT} L+	OUT	L-Channel Analog Current Output +
26	I _{OUT} L-	OUT	L-Channel Analog Current Output –
27	AGND2	_	Analog Ground
28	V _{CC} 3	_	Analog Power Supply, +5.0V

NOTES: (1) Schmitt-trigger input, 5V tolerant. (2) Tristate output.

Block Diagram



BDP-HD1

134

2

7.4 DISC / CONTENT FORMAT PLAYBACK COMPATIBILITY

BD-ROM playback

Blu-ray Disc is a next-generation video disc format featuring far higher disc capacity than conventional DVD. The higher capacity makes a whole range of new and enhanced features possible, such as support for high-definition video up to 1920 x 1080 pixels, high quality, surround sound audio, greater interactivity and richer content.

BD-ROM discs are commercially produced discs (Video Distribution format) that can contain movie and other video content, interactive content, enhanced menu features such as pop-up menus (press **MENU** during playback for these), full-color, high-definition animated buttons and animated menu transition effects, button sounds (sounds are played when menu buttons are selected or activated), high-definition bitmap subtitles supporting full-color images with frame-accurate animation effects up to full video frame rate, and so on.

While BD capacity is enough for most applications, the BD-ROM standard allows for content to be spread across several discs, removing the limit of one physical disc. Follow the on-screen instructions during playback when using these special kinds of discs.

BD-J application



esmertec

The BD-ROM specification supports Java for interactive content. The Java specification for BD-ROM is known as BD-J. This allows content providers to put games and other interactive material linked to specific titles on to BD-ROM discs. (This player does not support downloadable BD-J content, direct connection to the Internet or the retrieval of content through the Internet.)

Java and all Java-based marks are trademarks or registered trademarks of Sun Microsystems, Inc.

© 2000-2006 Esmertec AG

HDMI digital interface

The HDMI (High Definition Multimedia Interface) interconnect provides high quality digital audio and video, all from a single user-friendly connector. HDMI is the first consumer electronics interface to support uncompressed standard, enhanced, or high-definition video plus standard to multi-channel surround sound audio, all using one interface. You can easily connect to an HDMI-equipped AV receiver or audio-visual device for high quality audio and video.

HDMI, the HDMI logo and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC.

1080/60p and 1080/24p video output

5

This player supports a variety of video output resolutions, up to 1080 lines/60 frames per second, progressive (HDMI only), making it ideal for playing high-definition Blu-ray Discs.

Pure Cinema

There are two types of video signals: Video material, with a frame rate of 30 frames/second; and film material, that has a frame rate of 24 frames/second.

In PureCinema mode film material is converted to 60 frames/second progressive for an exceptionally clear picture.

High quality audio





Blu-ray supports DTS, DTS-HD (DTS-HD is played back as DTS), Dolby Digital, Dolby Digital Plus, Dolby TrueHD (Dolby Digital Plus and Dolby TrueHD are played back as Dolby Digital) and Linear PCM audio in up to eight channels (up to two channels for 24-bit/192 kHz audio). Connect this player to a surround-sound AV receiver for a true home theater experience.

Disc/content format playback compatibility

General disc compatibility

This player is compatible with a range of disc types (media) and formats. Compatible discs will usually feature one of the following logos on the disc and/or disc packaging. Note however that some disc types, such as recordable DVD or BD, may be in an unplayable format—see below for further compatibility information.

Blu-ray Disc (BD)



DVD-Video

DVD-R

DVD-R

DVD-RW

В

С

D

Ε

135

VIDEO

DVD R

- "Blu-ray Disc" and "Blu-ray Disc" are trademarks.
- **W** is a trademark of DVD Format/Logo Licensing Corporation.
- This player may not be able to play perfectly every disc that features one of the logos listed above. Please contact Pioneer if you find a disc that won't play properly.

TES.

Important

- This player is not compatible with BD-R/RE, DVD-R/RW (VR mode), DVD-Audio, DVD-RAM, CDs or disc types other than those listed above.
- This player is only compatible with NTSC discs.
- Do not use 8 cm disc adapters with this player. 8 cm discs can be played directly by placing then in the 8 cm disc depression in the center of the disc tray.

BD-ROM compatibility

- BD-ROM discs should conform to the BD-ROM Profile1.
- If a disc containing DTS-HD Bitstream audio is played, this
 player is only compatible with bitstream output or playback
 decoding of current DVD (DTS) material (sampling rate: 48 kHz
 max 5.1 ch.)
- If a disc containing Dolby Digital Plus or Dolby TrueHD audio is played, this player is only compatible with bitstream output or playback decoding of current DVD (Dolby Digital) material.
- This player cannot play 8 cm BD-ROM discs.

A DVD-R/RW compatibility

- This player is compatible with DVD-R/RW discs recorded in DVD-Video format.
- DVD-R/RW discs containing PC data can also be played. See below for file compatibility.
- Unfinalized DVD-R/RW discs and VR mode DVD-R/RW discs cannot be played in this player.

PC-created disc compatibility

Discs recorded using a personal computer may not be playable in this unit due to the settings of the application software used to create the disc. Check with the software publisher for more detailed information.

DualDisc playback

A DualDisc is a new two -sided disc, one side of which contains DVD content –video, audio, etc. –while the other side contains non-DVD content such as digital audio material.

The DVD side of a DualDisc will play in this product (excluding any DVD-Audio content).

The non-DVD, audio side of the disc is not compatible with this player.

It is possible that when loading or ejecting a DualDisc, the opposite side to that being played will be scratched. Scratched discs may not be playable.

For more detailed information on the DualDisc specification, please refer to the disc manufacturer or disc retailer.

Disclaimer Notice

C

D

This Blu-ray Disc player is not designed to play and cannot play the DVD portion of a hybrid disc.

File compatibility

- Compatible media: DVD-R, DVD-RW, media server on network (some formats may not be supported depending on the media server type).
- Even when they are in a supported format, some files may not play or display depending on the content.
- Even when playing a supported format, some functions may not operate properly depending on the content.

Video file compatibility

- · Windows Media Video (WMV)
 - WMV HD is supported
- MPEG-2 (PS/TS)
 - MP@HL
- MPEG-1

Audio file compatibility

- Windows Media Audio (WMA)
 - WMA9 (including variable bit-rate (VBR)), WMA9 Pro (up to 5.1 ch) are supported. WMA9 Voice and WMA Lossless are not supported
 - Sampling rates: up to 44.1kHz or 48 kHz (including WMA9 Pro)
 - Bit rate: up to 192 kbps (WMA constant bit-rate (CBR));
 up to 384 kbps (WMA9 variable bit-rate (VBR));
 up to 768 kbps (WMA9 Pro)

MPEG-1 Audio Layer 3 (MP3)

- Variable bit-rate (VBR) is supported
- Sampling rates: up to 32kHz, 44.1kHz or 48 kHz
- Bit rate: up to 320 kbps

WAVE (Linear PCM)

- Sampling rates: up to 44.1kHz or 48 kHz

Image file compatibility

JPEG

- Baseline JPEG and progressive JPEG/Exif are supported
- Resolution: up to 4096 x 4096 pixels

PNG

- Resolution: up to 4096 x 4096 pixels

• GIF

- Resolution: up to 4096 x 4096 pixels

File extensions

The following file extensions should be used with this player:

Video

.wmv .mpg .mpeg

Audio

.wma .mp3 .wav

Image

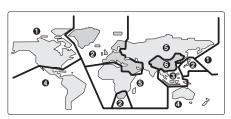
.jpg .jpeg .png .gif

Even when files have a supported file extension, some files may not play or display depending on the content or media server type.

DVD-Video regions

All commercially produced DVD movies (DVD-Video discs) carry a region mark on the case somewhere that indicates which region(s) of the world the disc is compatible with. This player also has a region mark, which you can find on the rear panel. Discs from incompatible regions will not play in this player. Discs marked **ALL** will play in any player.

The diagram below shows the various DVD regions of the world.



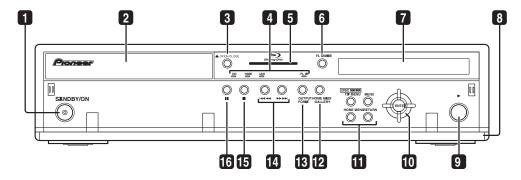
BD-ROM regions

Like DVD movies, BD movie discs (BD-ROM) also carry a region mark that indicates which region(s) of the world the disc is compatible with. This player also has a region mark, which you can find on the rear panel. Discs from incompatible regions will not play in this player. Discs marked **ALL** will play in any player.

The diagram below shows the various BD-ROM regions of the world.



Front panel



1 & STANDBY/ON

Press to switch the player on (the power indicator lights blue when the power is on) or into standby.

2 Disc tray

3 ▲ OPEN/CLOSE

Press to open or close the disc tray.

4 Indicators

- HD Lights when the video output is 720p, 1080i or 1080p (HDMI), or 720p or 1080i (component).
- HDMI Lights when an HDCP device is connected via HDMI.
- LAN Lights when there is an active local area network (LAN) connection.
- FL OFF Lights when the display and other indicators are switched off.

5 Blu-ray indicator

Lights when a BD disc is loaded.

6 FL DIMMER

Press to change the brightness of the display. When the display and other indicators are off, the **FL OFF** indicator (see above) lights.

7 Display

Shows disc status and playback information.

8 Flip-down cover

9 ▶

Press to start or resume disc playback.

10 ↑/↓/←/→ and ENTER

Use to navigate on-screen menus.

11 Menu navigation buttons

- MENU BD-ROM: Press to display/hide the pop-up menu. DVD-Video: Press to display the disc menu (if there is one).
- RETURN Press to return to a previous screen.
- DISC NAVIGATOR / TOP MENU Press to display the top menu of a BD-ROM or DVD-Video disc. When playing a DVD-R/RW or BD-R/RE disc, press to display/exit the Disc Navigator.
- HOME MENU Press to display the player's Home Menu, from which you can access most of the player's functions.

12 HOME MEDIA GALLERY

Press to access the Home Media Gallery screen.

13 OUTPUT FORMAT

Press to switch the output format over HDMI and component video outputs. See *Changing the video output format* .

14 Skip/scan buttons

- DDD—Press to jump to the next chapter, track, etc. Press and hold for fast forward scanning
- I < < <-> Press to jump back to the beginning of the current chapter, track, etc. then to previous chapters, tracks, etc. Press and hold for fast reverse scanning.

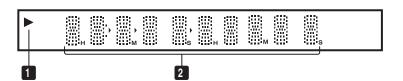
15 ■

Press to stop the disc (you can resume playback by pressing ▶(play)).

16 II

Press to pause playback. Press again to restart.

Front panel display



1 ▶

Lights during playback of a disc or file.

2 Character display

5

Shows various playback information—disc time, chapter and title number, etc.

BDP-HD1

137

В

С

D

Ε

В

С

D

Ε

F

Connect the supplied power cord here, then plug into a power outlet.

2 CONTROL IN

Use to control this player from the remote sensor of another Pioneer

component with a **CONTROL OUT** terminal and bearing the mark. Connect the CONTROL OUT of the other component to the CONTROL IN of this player using a mini-plug cord .

HDMI OUT

HDMI output providing a high quality interface for digital audio and video .

Ethernet port for 10base-T (10 Mbps) or 100base-TX (100 Mbps) network connection.

5 VIDEO and S-VIDEO OUT

Video output (composite) that you can connect to your TV or AV receiver using the supplied video cable.

S-Video output that you can use instead of the VIDEO OUT jacks .

6 COMPONENT VIDEO OUT

High quality video output for connection to a TV, monitor or AV receiver that has component video inputs.

Connect using a commercially available three-way component video cable.

7 DIGITAL AUDIO OUT - OPTICAL / COAXIAL

Digital audio outputs for connection to a PCM, Dolby Digital, DTS and/ or MPEG-compatible AV receiver .

8 AUDIO OUT (5.1ch)

Multichannel (5.1ch) analog audio outputs for connection to an AV receiver with multichannel analog audio inputs.

AUDIO OUT (2ch)

Stereo analog audio outputs for connection to your TV, AV receiver or stereo system.

10 IR IN

Jack for an external IR (infrared) remote control receiver .

11 IR RECEIVER switch

Switch to the setting compatible with your external IR remote control receiver.



- When connecting this player to your TV, AV receiver or other equipment, make sure that all components are switched off and unplugged.
- · Youmay find it useful to have the manuals supplied with your other components handy when connecting this player.

2

BDP-HD1

1 也 STANDBY/ON

Press to switch the player on or into standby.

2 ▲ OPEN/CLOSE

Press to open or close the disc tray.

3 BLUE/ RED/ GREEN/ YELLOW

Use to navigate BD-ROM menus.

Number buttons

Use to enter title, track numbers, etc.

CLEAR: Press to clear a numeric entry, etc.

5 DISPLAY

Press to display information about the disc playing.

Press to change the brightness of the display. When the display and other indicators are off, the FL OFF indicator (see above) lights.

OUTPUT FORMAT

Press to switch the output format over HDMI and component video outputs.

8 HOME MEDIA GALLERY

5

Press to display the Home Media Gallery screen .

9 DISC NAVIGATOR / TOP MENU

Press to display the top menu of a BD-ROM or DVD-Video disc. When playing a DVD-R/RW disc, press to display/exit the Disc Navigator.

10 MENU

BD-ROM: Press to display/hide the pop-up menu. DVD-Video: Press to display the disc menu (if there is one).

11 \uparrow , \downarrow , \leftarrow , \rightarrow and ENTER

Use to navigate on-screen displays and menus. Press ENTER to select an option or execute a command.

Press to display the player's Home Menu, from which you can access most of the player's functions.

13 RETURN

Press to return to a previous screen.

14 Playback controls

✓ / ►► : Press to start reverse/forward scanning.

: Press to start or resume playback.

II : Press to pause playback; press again to restart.

■ : Press to stop the disc (you can resume playback by pressing ► (play)).

ZOOM: Press to zoom the screen when displaying a moving or still image.

I◄ ▶►I: Press to jump to the start of the previous / next chapter / track.

◄II II► : Use for slow motion and step frame .

Press to select the audio channel or language.

16 SUBTITLE

Press to select a subtitle display.

17 PLAY MODE

Press to change the Play Mode (repeat play, for example).

18 ANGLE

Press to change the camera angle during BD or DVD movie multiangle scene playback.

During photo slideshow playback, press to rotate the current photo 90°.

19 TV CONTROL buttons

See also Setting up the remote to control your TV.

Ů : Press Ů to turn the TV on or into standby.

VOLUME +/- : Use to adjust the volume.

CHANNEL +/- : Use to select TV channel.

INPUT SELECT: Press to change the input function of the TV.

BDP-HD1

139

8

Α

В

С

D

Ε

■ Jigs list

Name	Jig No.	Remarks
Service Remote Control Unit	GGF1381	adjustment, diagnosis
ID Data Disc for Blu-ray player	GGV1306	ID data setting
Extension Cable	GGD1437	Diagnosis of MAIN Assy
Extension Board	GGF1533	Diagnosis of MAIN Assy
DVD Test Disc (DVD-Video)	GGV1025	Check of DVD-Video
Tray Ejection Rod	GGF1529	Diagnosis and Firmwave Update

3

В

С

D

Ε

F